

# Compal Confidential

## EL432/EL532

### M/B Schematic Documents

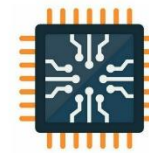
#### AMD Picasso FP5 APU with DDR4

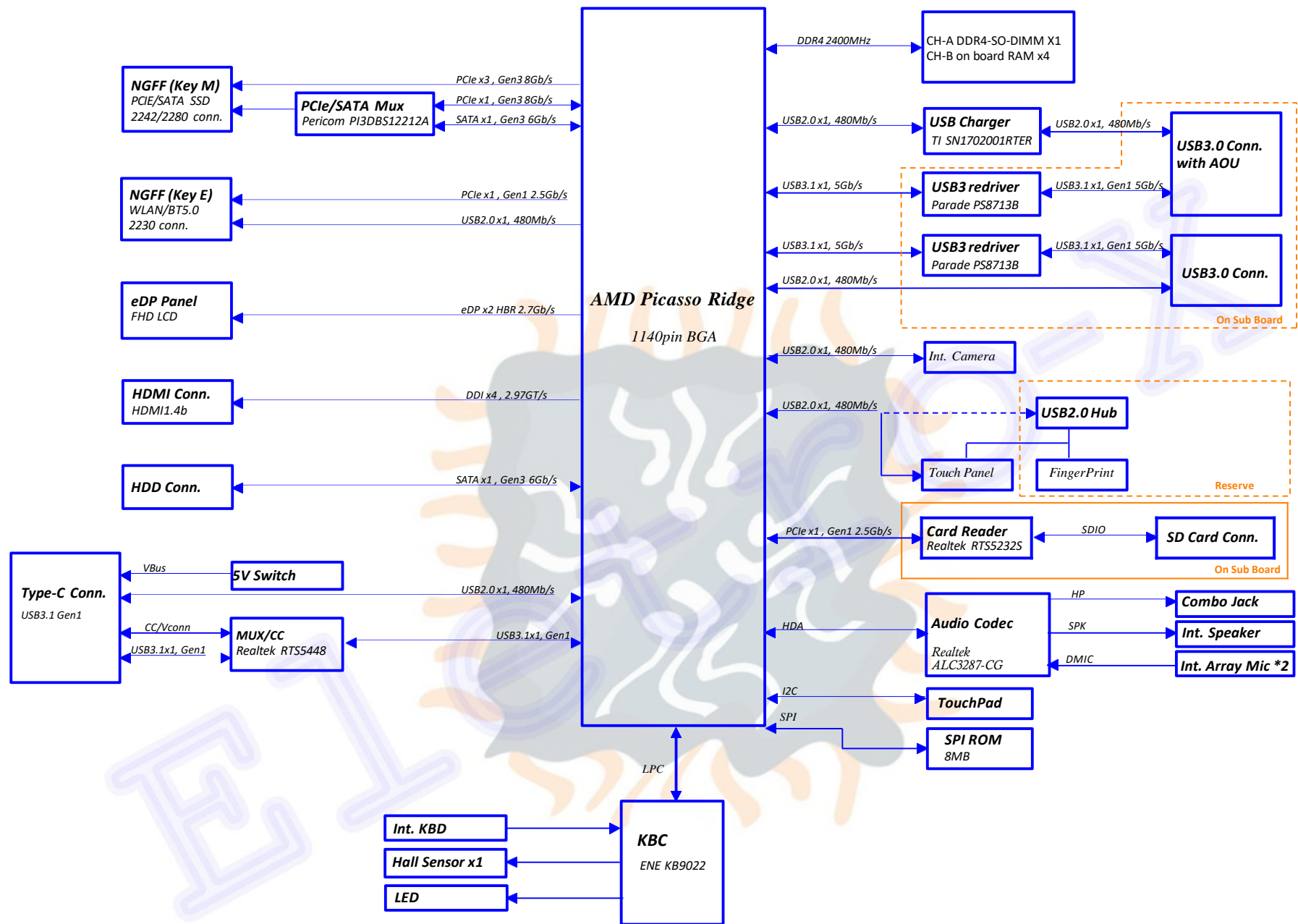
#### LA-H131P

#### 2018-11-05

#### Rev : 0.4

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Power Sequence

Boot

Shut  
Down

EC Pin 110 Input

EC Pin 112 Output

AC Plug

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 123 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Output

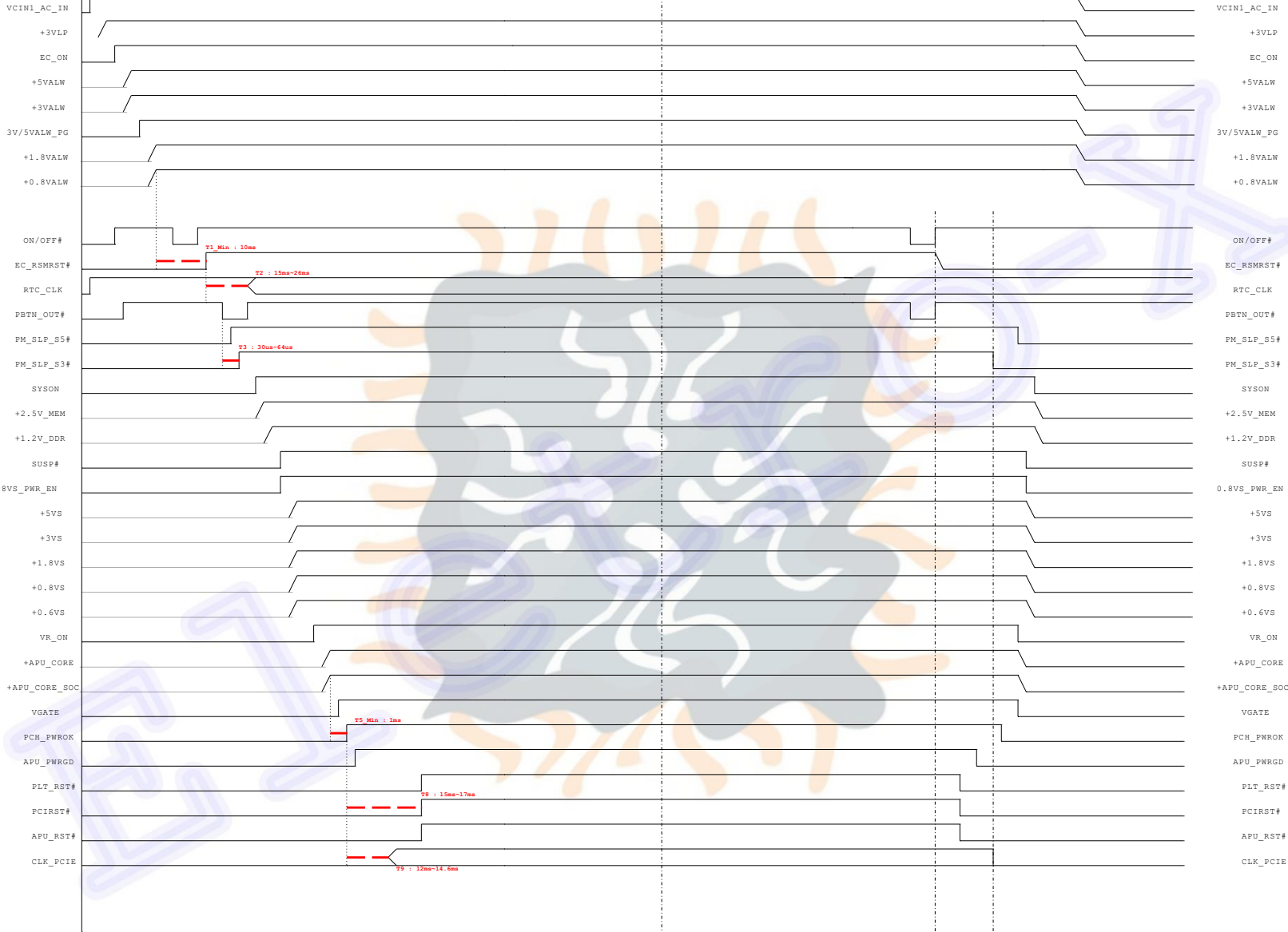
EC Pin 99 Output

EC Pin 121 Output

EC Pin 36 Input

EC Pin 32 Output

EC Pin 13 Input



## Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.8VALW	0.95V always on power rail	ON	ON	ON
+0.8VS	0.95V switched power rail	ON	OFF	OFF
+1.2V_DDR	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V_MEM	2.5V power rail for DDR	ON	ON	OFF
+0.6VS_VTT	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOM STRUCTURE	DESCRIPTION
14@	14" Only Components
15@	15" Only Components
OBR@	On Board RAM SKU Only
NO_OBR@	No On Board RAM SKU Only
SDP@	Memory Down - SDP Package
DDP@	Memory Down - DDP Package
SINGLE_MIC@	MIC Select Strap (1 MIC)
MULTI_MIC@	MIC Select Strap (2 MIC)
KBL@	Keyboard Backlight

## BOM STRUCTURE

BOM STRUCTURE	DESCRIPTION
Ryzen5_PR@	Ryzen5 CPU (PR Sample)
Ryzen7_PR@	Ryzen7 CPU (PR Sample)
45@	HDMI Logo
14_DAZ_R0@	14" DAZ (Rev0 PCB)
15_DAZ_R0@	15" DAZ (Rev0 PCB)
X4E@	43J X4E Level
X76RAM@	On Board RAM X76 Resistors
S4G_MD@	On Board RAM (Samsung 4GB)
H4G_MD@	On Board RAM (Hynix 4GB)
M4G_MD@	On Board RAM (Micron 4GB)
HDT@	HDT Debugging
EMI@	EMI Components
ESD@	ESD Components
RF@	RF Components
TS@	Touch Screen

BOM STRUCTURE	DESCRIPTION
Ryzen3_PC@	Ryzen3 CPU (PC Sample)
Ryzen3_PR@	Ryzen3 CPU (PR Sample)
Ryzen5_PC@	Ryzen5 CPU (PC Sample)
Ryzen7_ES@	Ryzen7 CPU (ES Sample)
Ryzen7_PC@	Ryzen7 CPU (PC Sample)
@	Un-Mount Components
EMI@	EMI Un-Mount Components
ESD@	ESD Un-Mount Components
20V_PRTCT@	5448 EXT Voltage Protection
FP@	Finger Printer (Reserved)
ME@	ME Components
EX_THM@	Thermal Sensor
HUB@	USB2.0 HUB
DA_R0@	PCB Part Number (Rev0 PCB)
DA_R1@	PCB Part Number (Rev1 PCB)
14_DAZ_R1@	14" DAZ (Rev1 PCB)
15_DAZ_R1@	15" DAZ (Rev1 PCB)
RD@	USB3.0 Re-Driver BOM
TI@	TI Re-Driver Only
PARADE@	Parade Re-Driver Only
PERICOM@	Pericom Re-Driver Only
X76_TI@	TI Re-Driver X76 Level
X76_PARADE@	Parade Re-Driver X76 Level
X76_PERICOM@	Pericom Re-Driver X76 Level

## SMBUS Control Table

	SOURCE	APU	BATT	EC	SODIMM	WLAN
EC_SMB_CK1 EC_SMB_DA1	9022 +3VALW	X	V +3VALW	V +3VALW	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X +3VS		X
EC_SMB_CK2 EC_SMB_DA2	9022 +3VS	V +1.8VS	X	V +3VALW	X	X

## EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011x b	16H
Charger	0001 0010 b	12H

## EC SM Bus2 address

Device	Address	HEX
APU	1001 100X b	98H

## APU SM Bus address

SM Bus0	Device	Address	HEX
	DDR DIMM1	1010 001Xb	A2H

## APU I2C Bus address

I2C 3	Device	Address
	Touch Pad (Synaptics) \$2C	
	Touch Pad (Elan) 0X15	

## USB3.0 Port (USB\_0)

PORT	FUNCTION
0	Type-C
1	Sub/B USB3.0 Type-A
2	Sub/B USB3.0 Type-A
3	
4	

## USB2.0 Port

PORT	FUNCTION
0	Type-C
1	Sub/B USB3.0 Type-A
2	Sub/B USB3.0 Type-A
3	Camera
4	USB2.0 Hub
5	Bluetooth

## USB2.0 Hub

PORT	FUNCTION
1	Touch Screen
2	Finger Printer

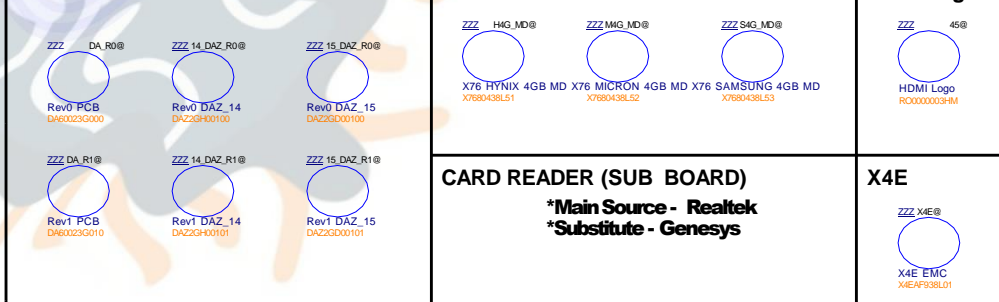
## GPP Port

PORT	FUNCTION
GPP0	
GPP1	
GPP2	SSD (PCIe x4)
GPP3	
GPP4	Card Reader (PCIe x1)
GPP5	WLAN (PCIe x1)
GPP6	SSD (SATA x1)
GPP7	HDD (SATA x1)

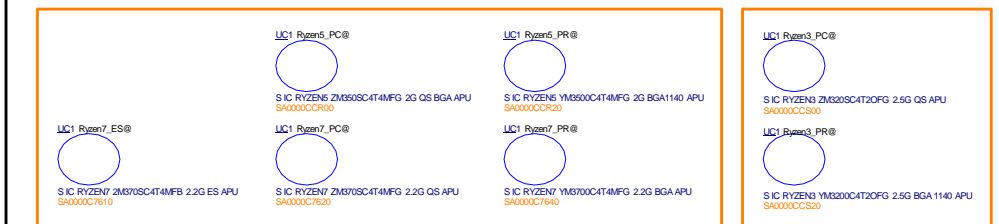
## Display Port

PORT	FUNCTION
0	eDP
1	HDMI

## PCB



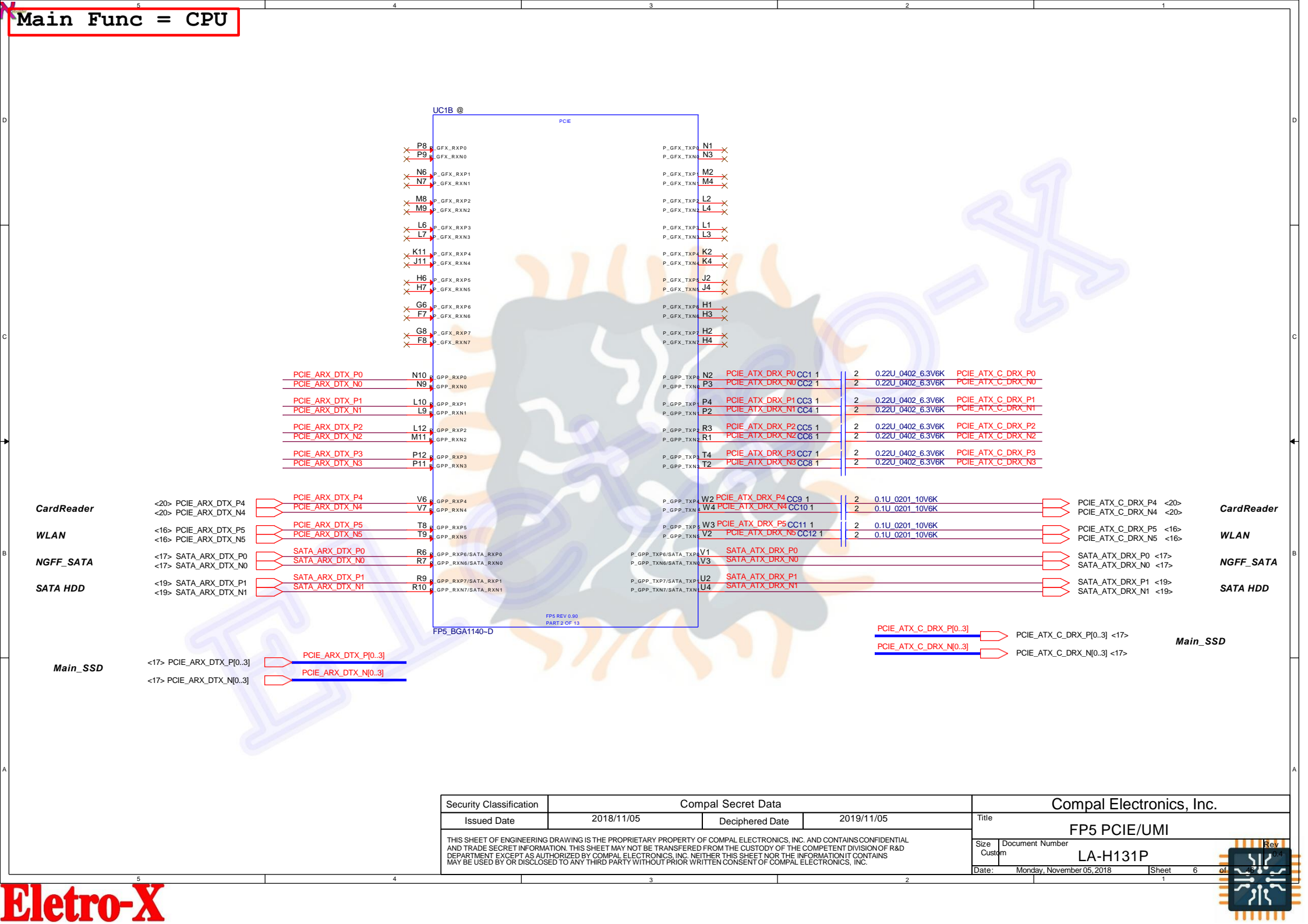
## CPU



TYPE1		TYPE2	
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**Main Func = CPU**

UC1B @

PCIE

FP5\_BGA1140-D

FP5 REV 0.90  
PART 2 OF 13

CardReader

WLAN

NGFF\_SATA

SATA HDD

Main\_SSD

Security Classification

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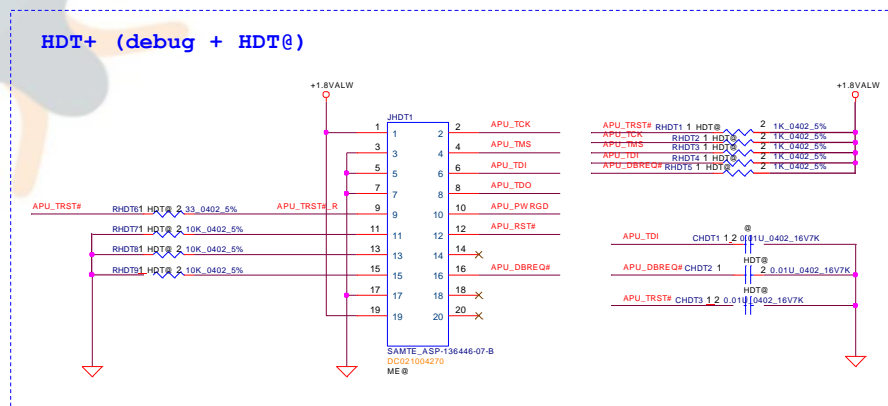
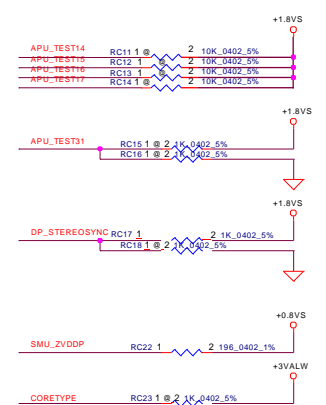
FP5 PCIE/UMI

LA-H131P

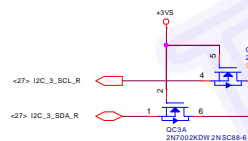
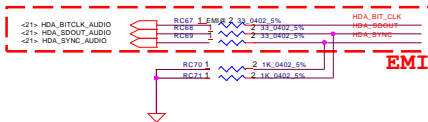
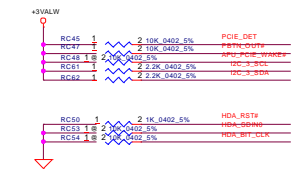
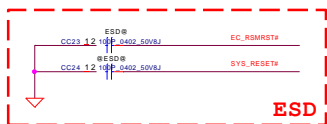
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			Standard/Document Number	LA-H131P
			Customer	
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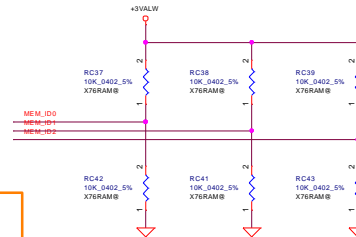


Capacit y	Description	X76	PART NUMBER R1	PART NUMBER R3
	WITHOUT ON-BOARD RAM	N/A	N/A	N/A
	SAMSUNG 2666MHz K4A8G16SWC-BCTD	X7680438L53	SA0000B8F00	SA0000B8F10
	MICRON 2666MHz MT40A512M16LY-075E	X7680438L52	SA0000ARD20	SA0000ARD30
	HYNIX 2666MHz H5AN8GNCJR-VKC	X7680438L51	SA0000BMN00	SA0000BMN10
4GB	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	N/A

Capacit y	Description	AGPIO11 MEM ID2	AGPIO9 MEM ID1	AGPIO6 MEM ID0
	WITHOUT ON-BOARD RAM	0	0	0
	N/A	0	1	0
	N/A	0	1	1
	N/A	1	0	0
4GB	SAMSUNG 2666MHz K4A8G16SWC-BCTD	1	0	1
	MICRON 2666MHz MT40A512M16LY-075E	1	1	0
	HYNIX 2666MHz H5AN8GNCJR-VKC	1	1	1

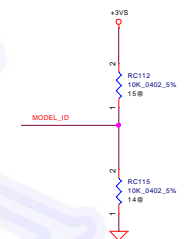
- SCL41 NO\_OBR#
- SCL42 NO\_OBR#
- SCL43 NO\_OBR#
- SCL44 NO\_OBR#

No On Board RAM Straps (NO\_OBR@)

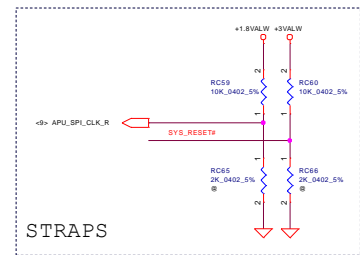
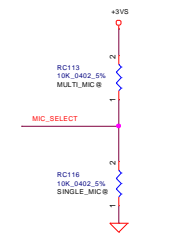


ON BOARD RAM ID

Function	MODEL ID
S340-14	AGPIO89
S340-15	0

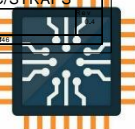


Function	MIC SELECT
MIC	0
MIC	1



STRAPS	DEFINITION
SPI_CLK	1: Use 48MHz Crystal Clock and Generate both internal and external cs (Default) 0: Use 100MHz PCIe clock as reference clock and generate internal clocks only
SYS_RST#	1: Normal reset mode (Default) 0: short reset mode

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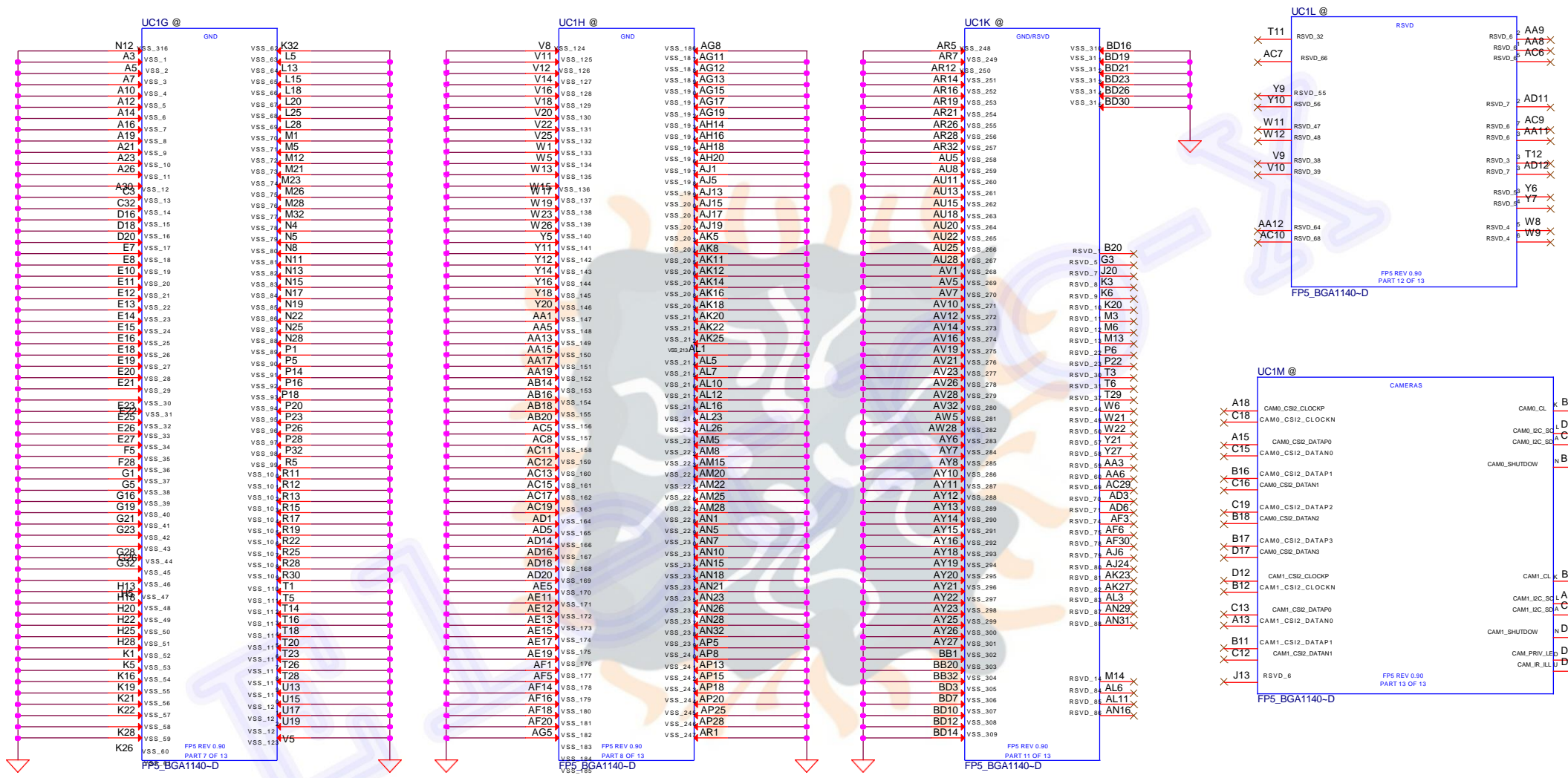




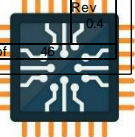




Main Func = CPU

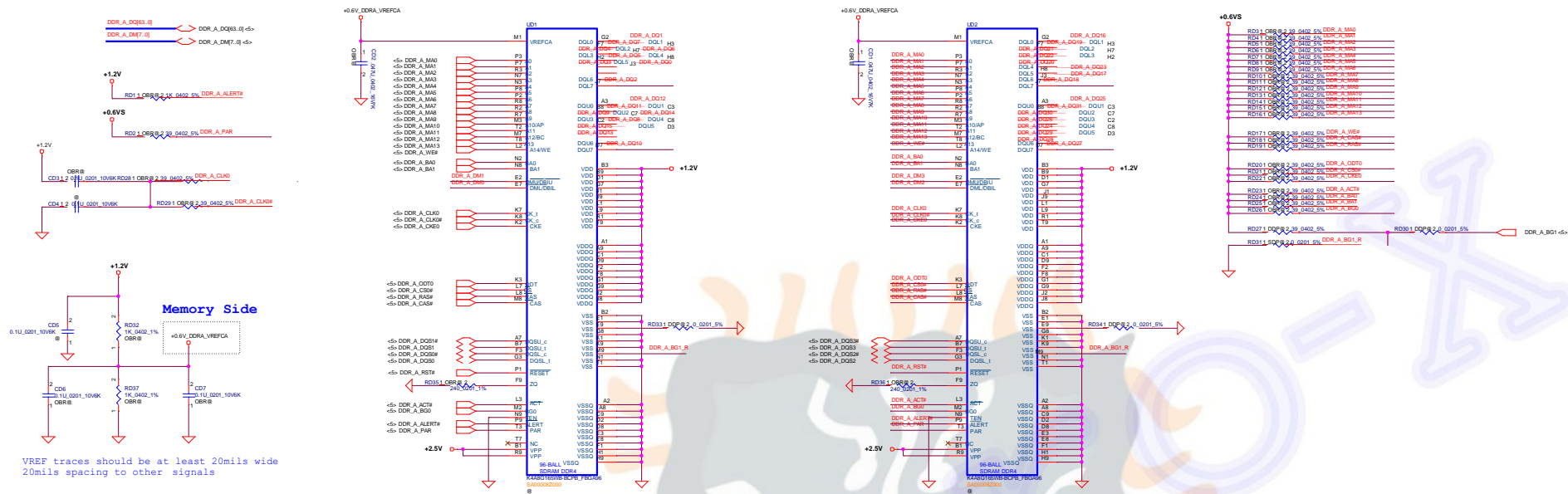


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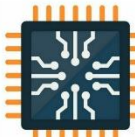
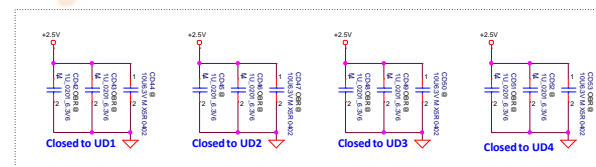
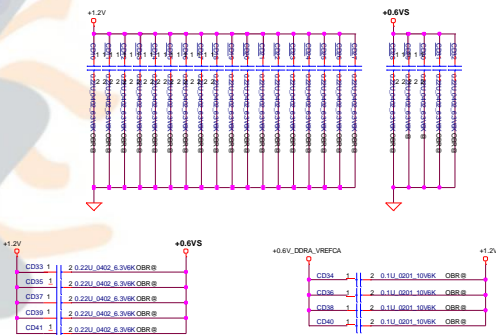




# DDR4 - MEMORY DOWN (MEMORY CHANNEL A, x16 x4 PCS)

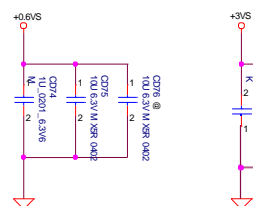
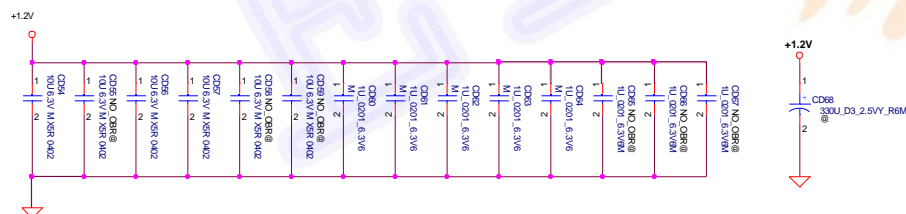
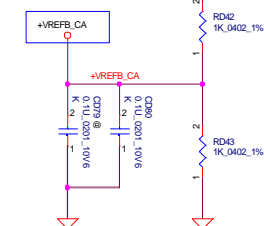
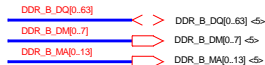


## DRAM DOWN DECOUPLING

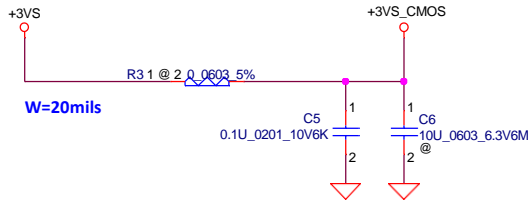




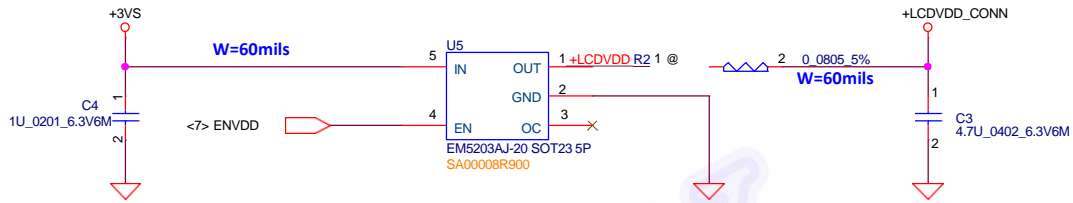
# Eletro-X



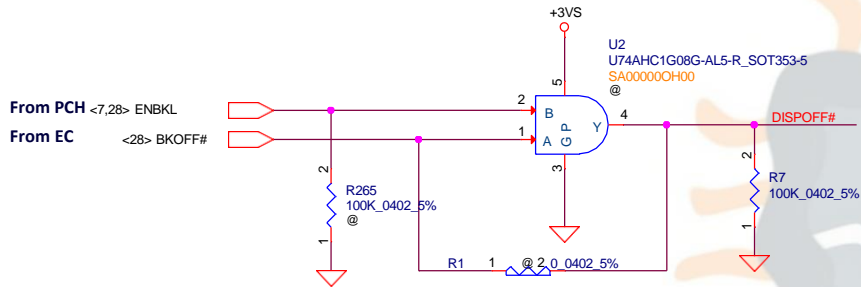
CAMERA POWER CIRCUIT



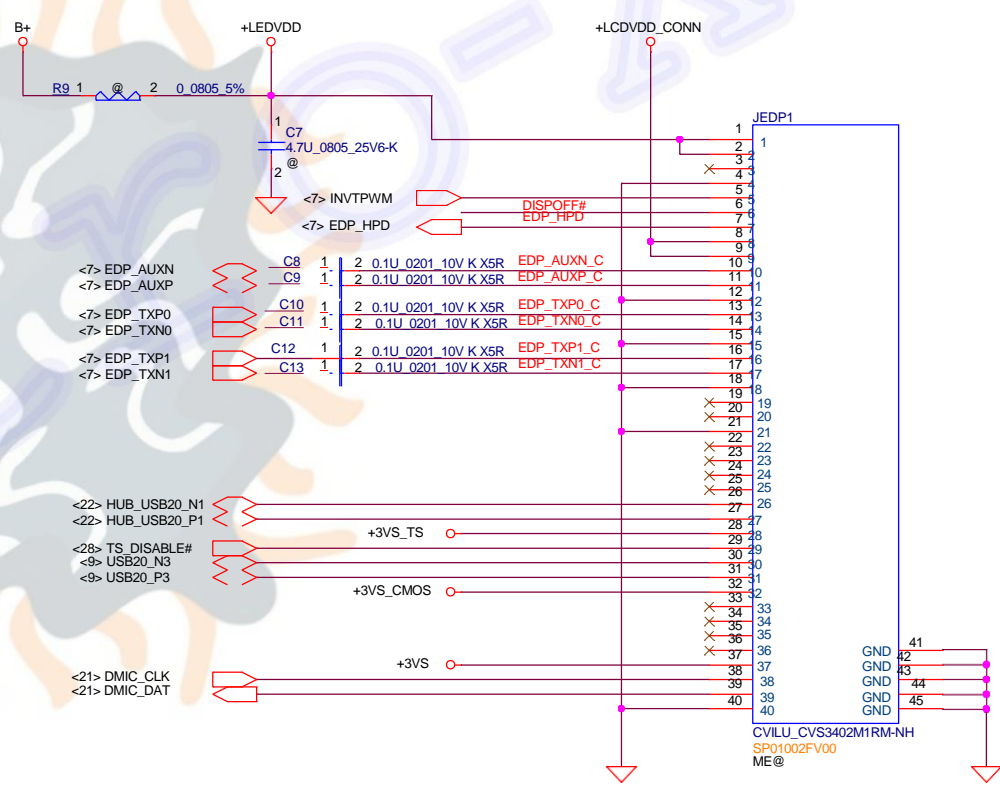
LCD POWER SWITCH



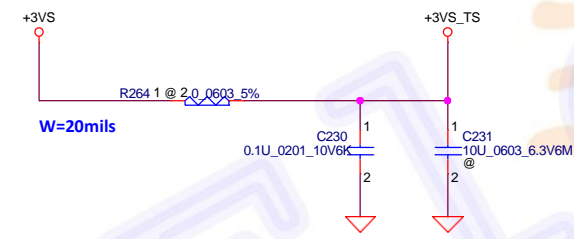
DISPLAY OFF



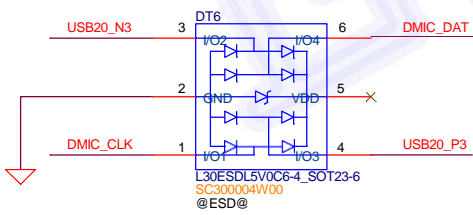
EDP CONNECTOR



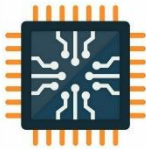
TOUCH SCREEN POWER CIRCUIT



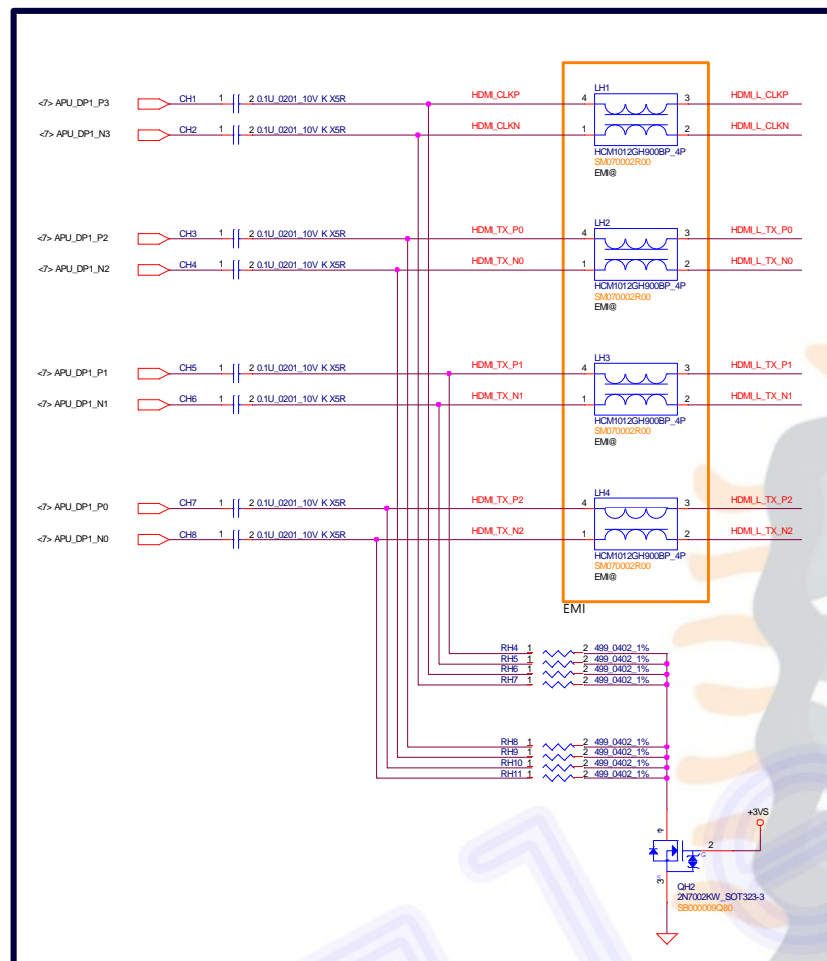
ESD COMPONENTS



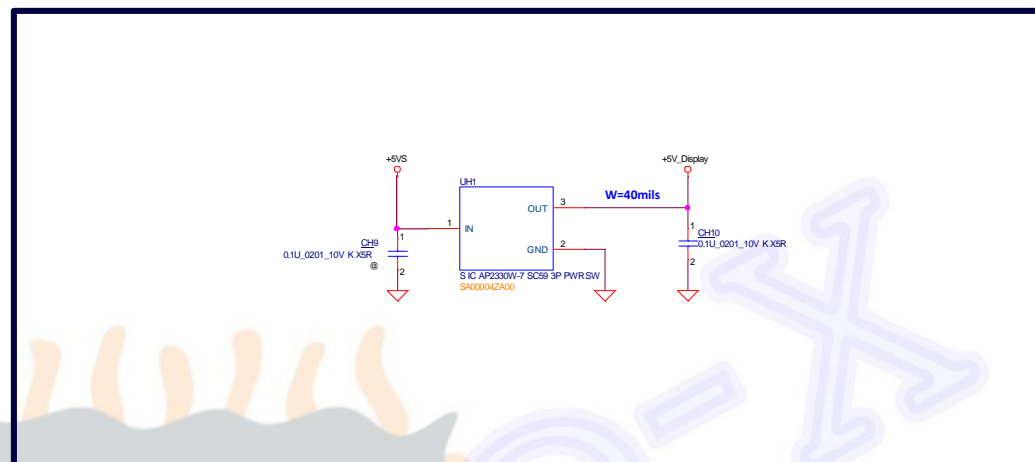
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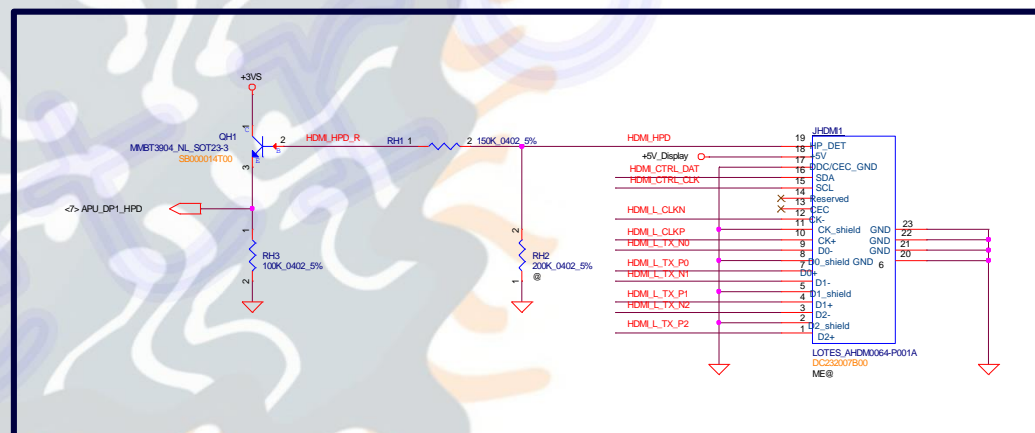
## HDMI DIFFERENTIAL SIGNALS



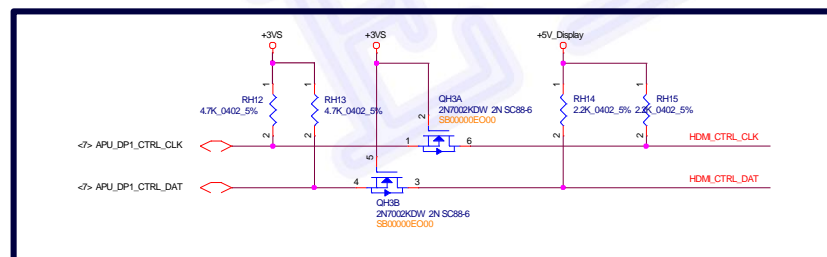
## HDMI POWER CIRCUIT



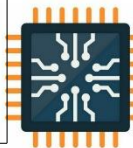
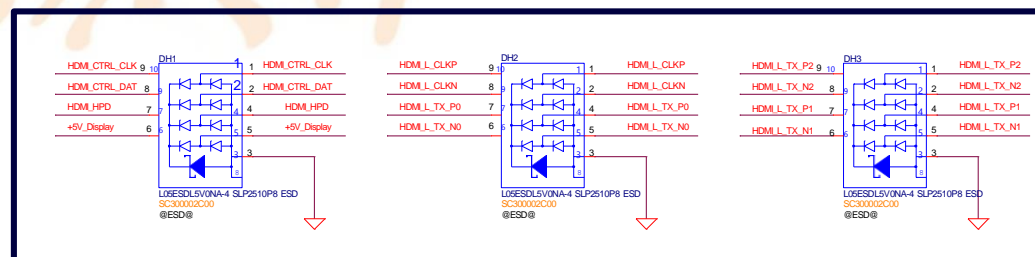
## HDMI CONNECTOR



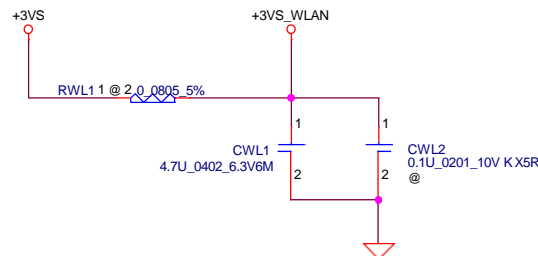
## AUX LEVEL SHIFTER



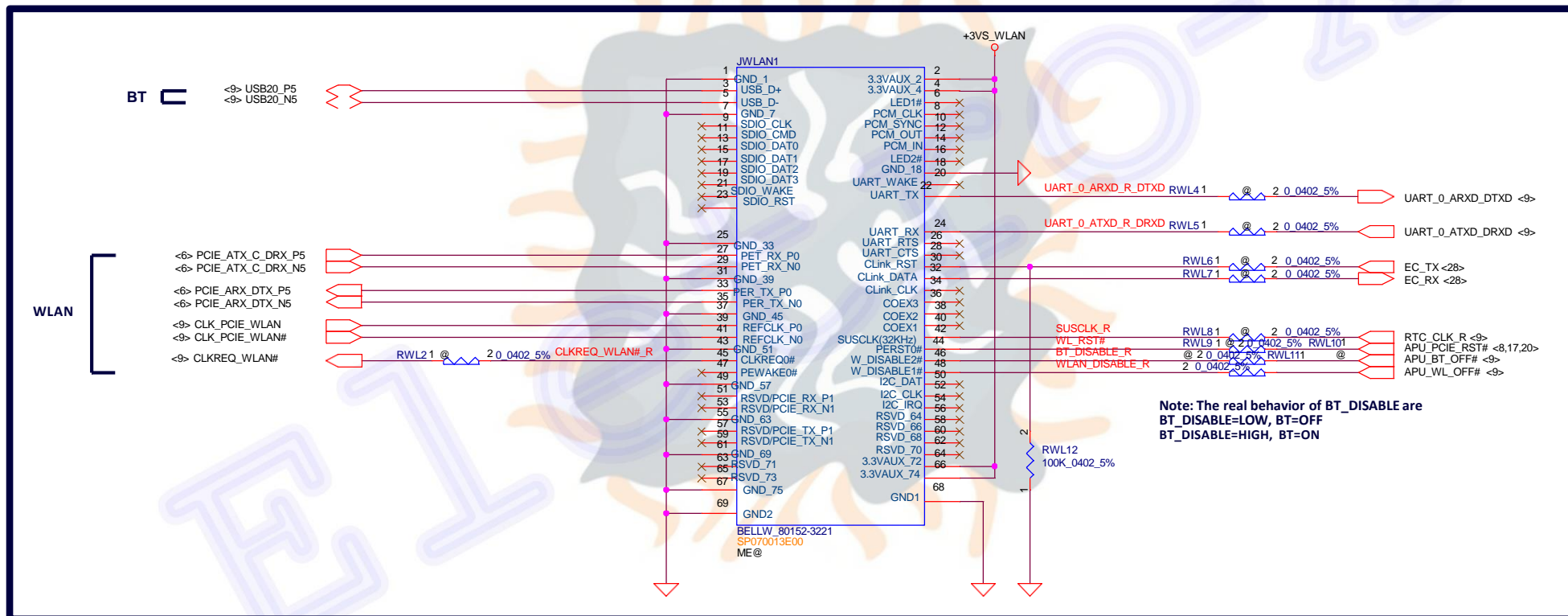
## ESD COMPONENTS



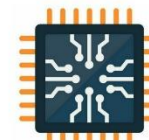
# WLAN POWER CIRCUIT



# NGFF - WLAN / BT CONNECTOR (KEY-E)

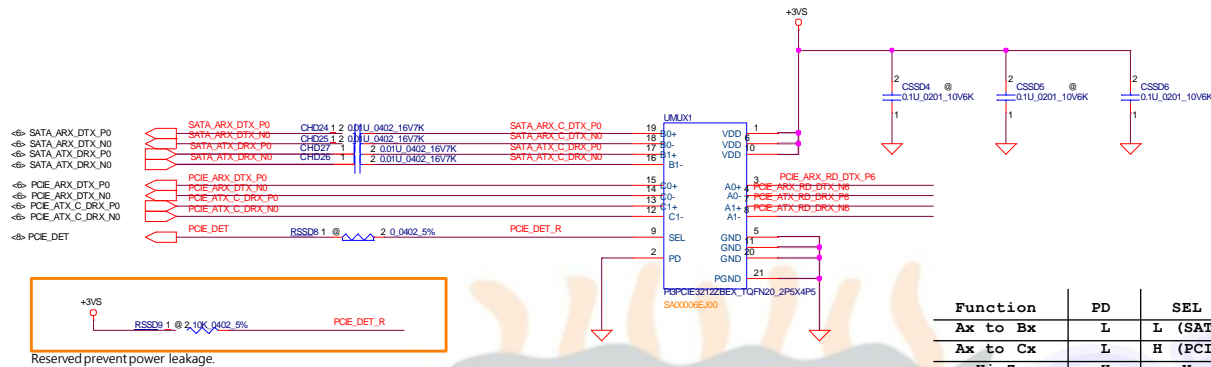


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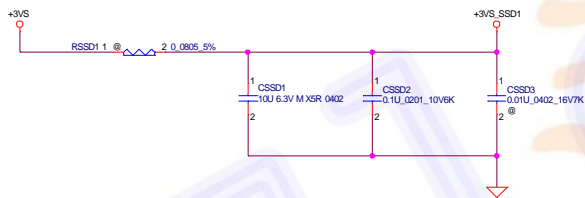


## PCIE / SATA MUX (PERICOM PI3PCIE3212ZBEX)

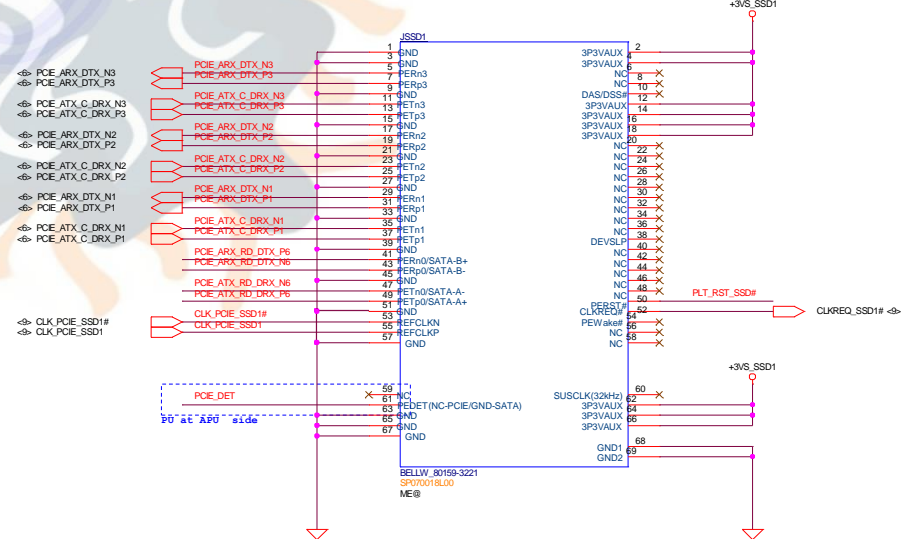


Function	PD	SEL
Ax to Bx	L	L (SATA)
Ax to Cx	L	H (PCIe)
Hi-Z	H	X

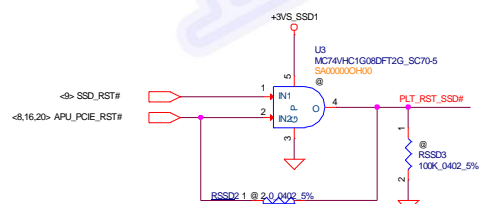
## SSD POWER CIRCUIT



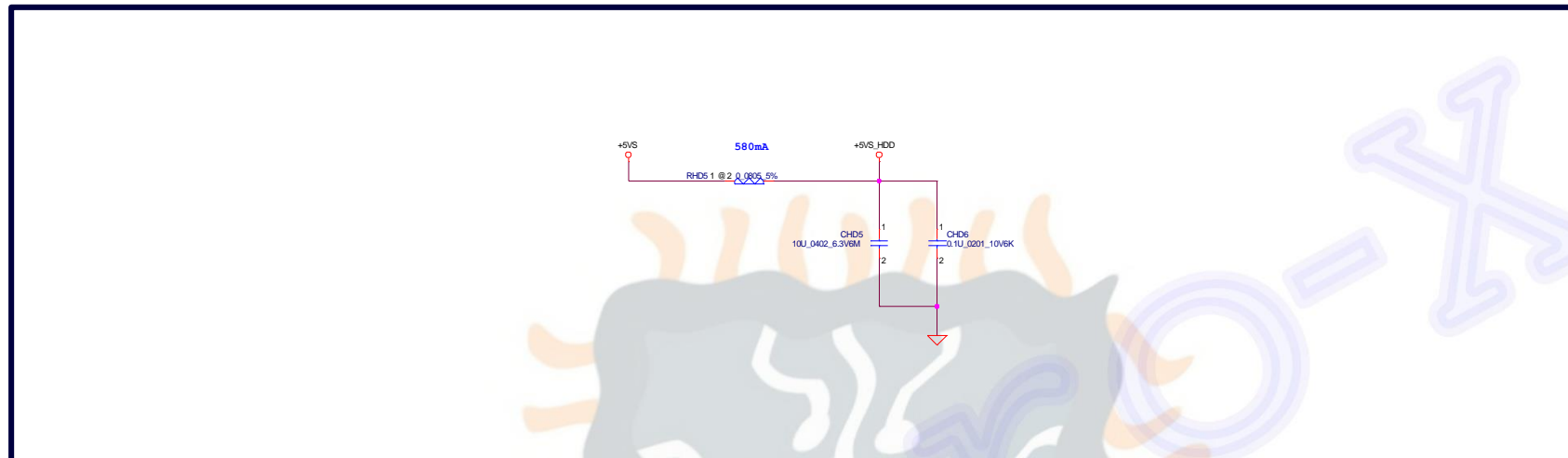
## NGFF - SSD CONNECTOR (KEY-M)



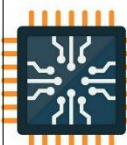
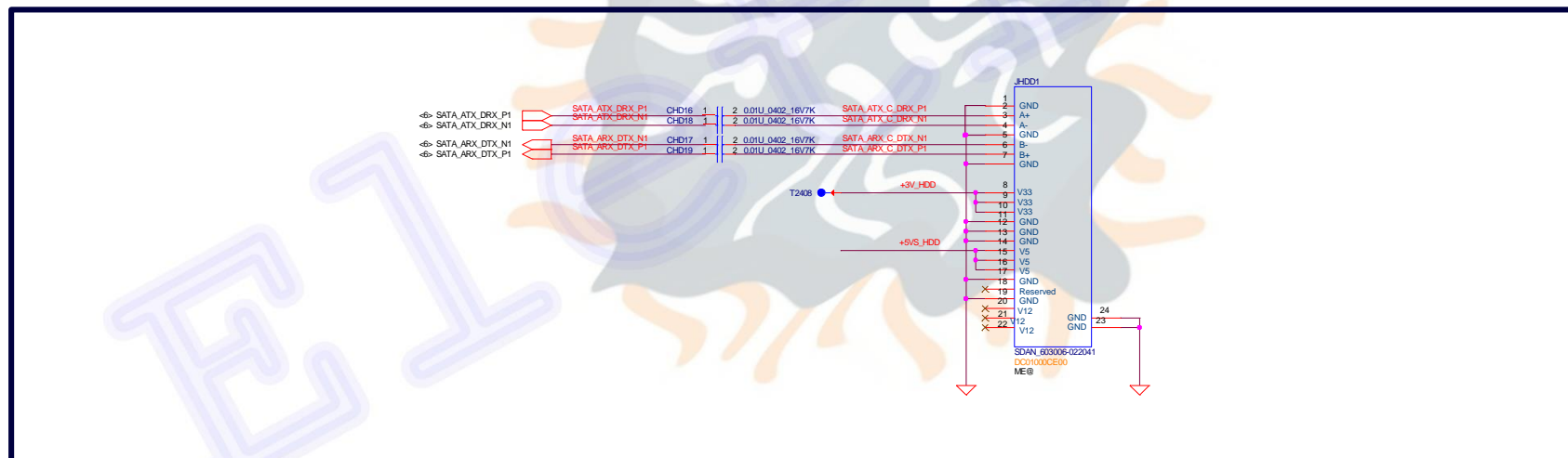
## PCIE RESET



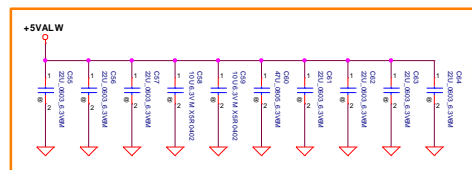
## HDD POWER CIRCUIT



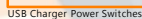
## HDD CONNECTOR



## USB Charger For Sub Board USB3.0 Connector



Improve +5VALW Power Ripple



## IO Connector

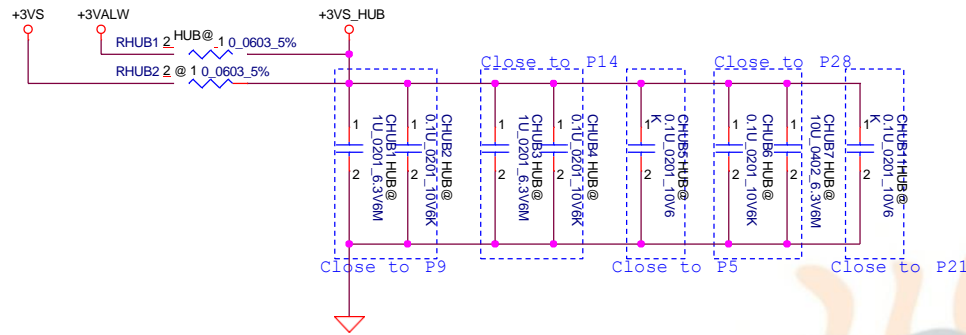
## USB Power Switch For Sub Board USB3.0 Connector (Non-AOU Port)



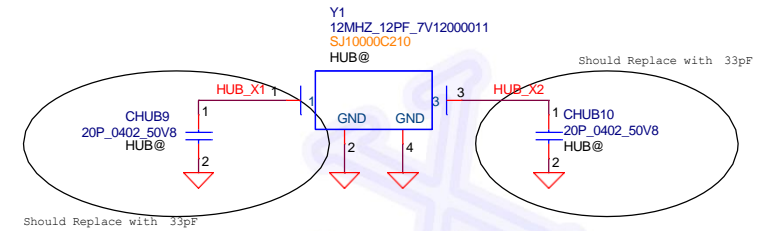




# USB HUB POWER CIRCUIT



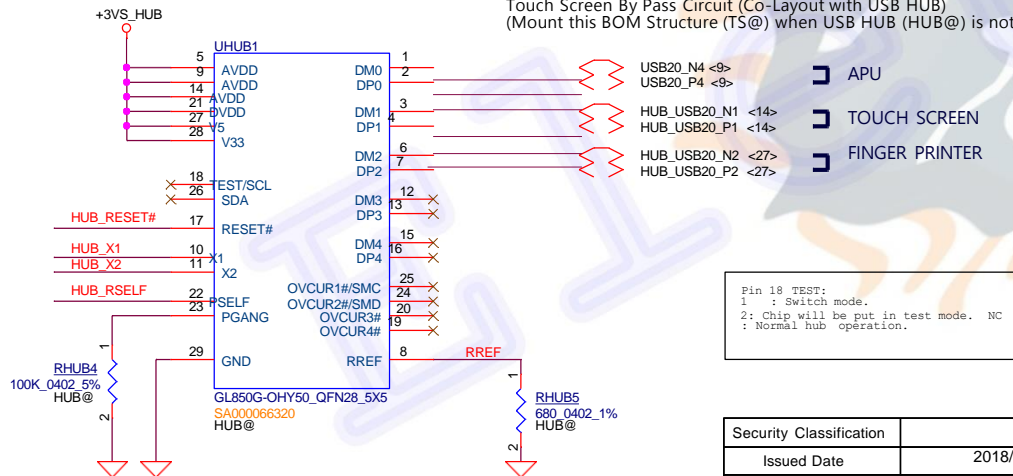
# CRYSTAL (12 MHz)



# USB 2.0 HUB (GENESYS GL850G-OHY50)

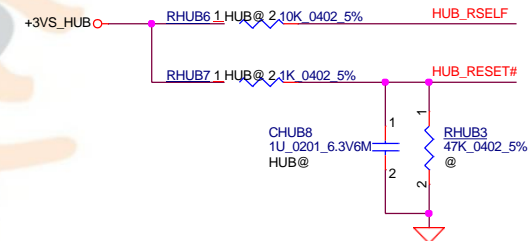
USB20\_TS\_N1 RHUB101 TS@ 2.0\_0201 5% USB20\_N4  
 USB20\_TS\_P1 RHUB111 TS@ 2.0\_0201 5% USB20\_P4 USB20\_TS\_N1  
 RHUB121 TS@ 2.0\_0201 5% HUB USB20\_N1  
 USB20\_TS\_P1 RHUB131 TS@ 2.0\_0201 5% HUB USB20\_P1

Touch Screen By Pass Circuit (Co-Layout with USB HUB)  
 (Mount this BOM Structure (TS@) when USB HUB (HUB@) is not used)



Pin 18 TEST:  
 1 : Switch mode.  
 2: Chip will be put in test mode. NC  
 : Normal hub operation.

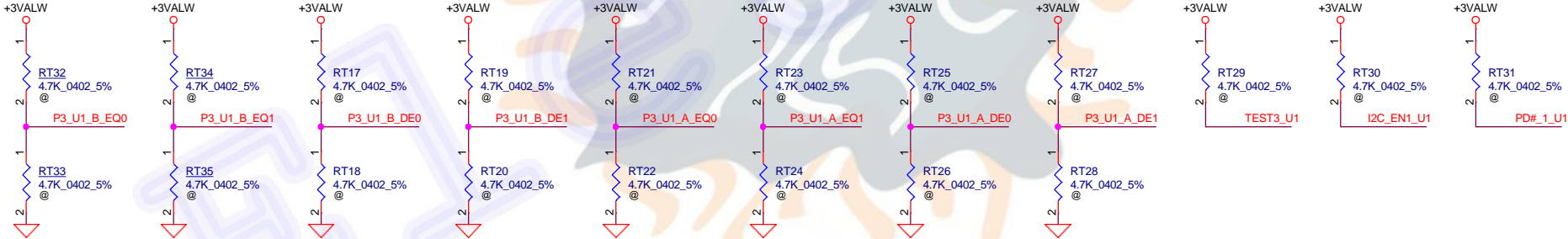
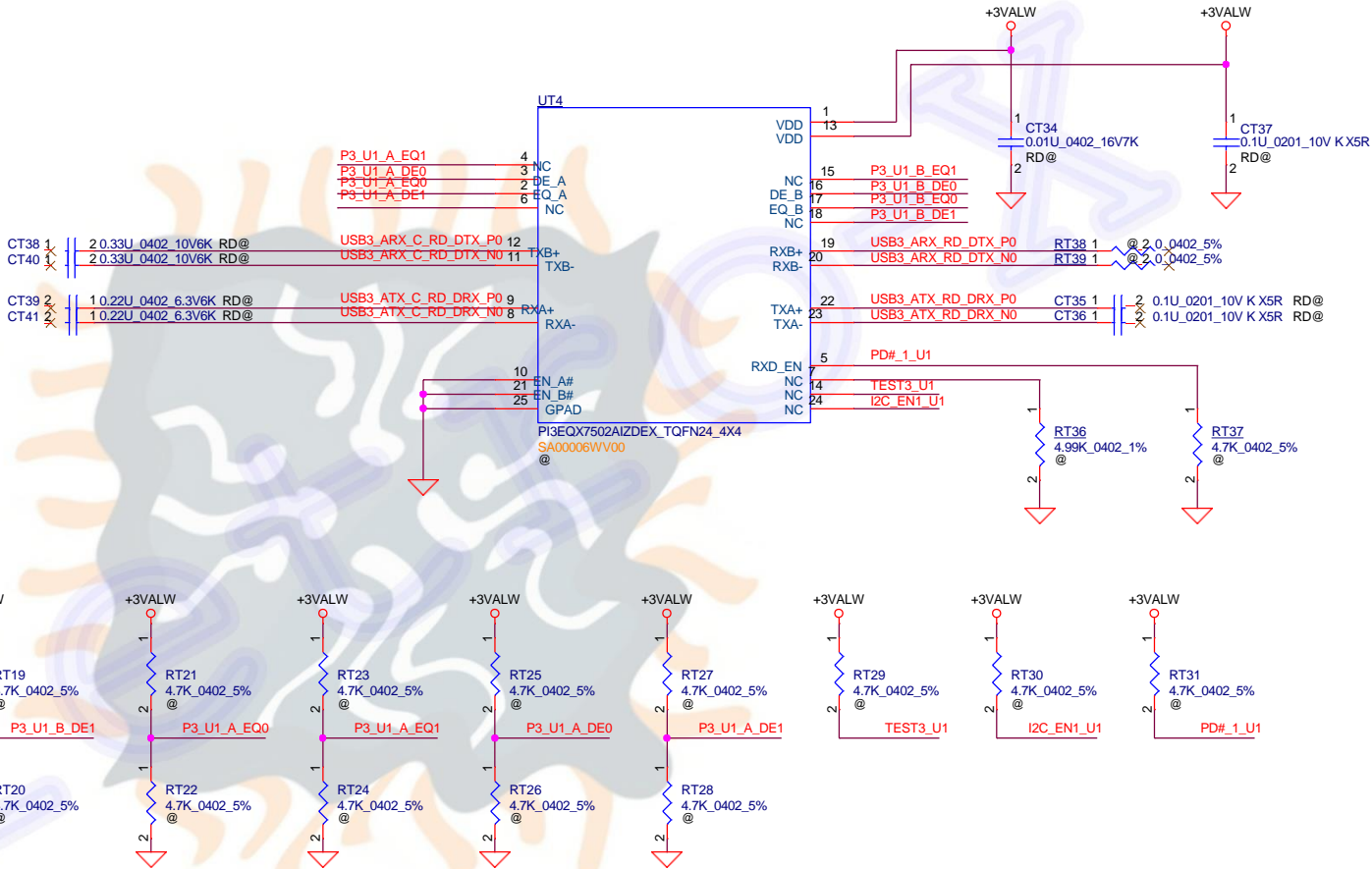
# HUB MISC.



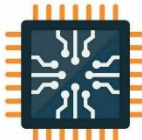
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Issued Date	2018/11/05	Deciphered Date	2019/11/05	Title	
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Size	Document Number	LA-H131P		Rev	0.4
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TI@	UT4 TI@ SN65LVPE512RGE R SA00008M500	RT28 TI@ 0_0402_5%	RT20 TI@ 0_0402_5%	RT33 TI@ 4.7K_0402_5%	RT35 TI@ 4.7K_0402_5%	RT18 TI@ 4.7K_0402_5%
PARADE@	UT4 PARADE@ PS8713BTQFN24GTR2-A2 SA00005OR30	RT23 PARADE@ 4.7K_0402_5%				
PERICOM@	UT4 PERICOM@ PI3EQX7502AIZDEX_TQFN24 SA00006WV00	RT33 PERICOM@ 4.7K_0402_5%	RT22 PERICOM@ 4.7K_0402_5%	RT26 PERICOM@ 4.7K_0402_5%		

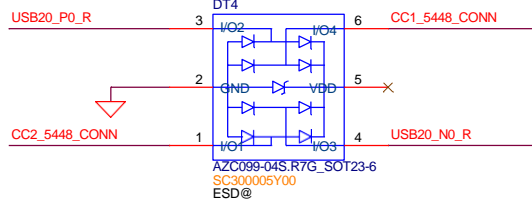
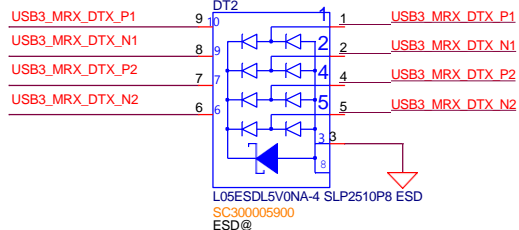
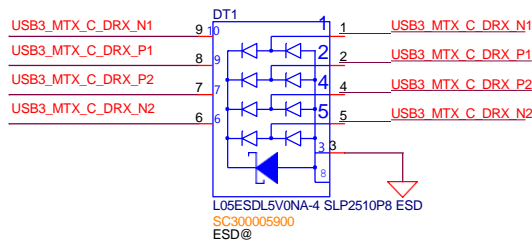


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						Size		Document Number		Rev	
						B		LA-H131P		0.4	
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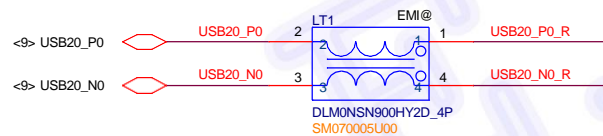




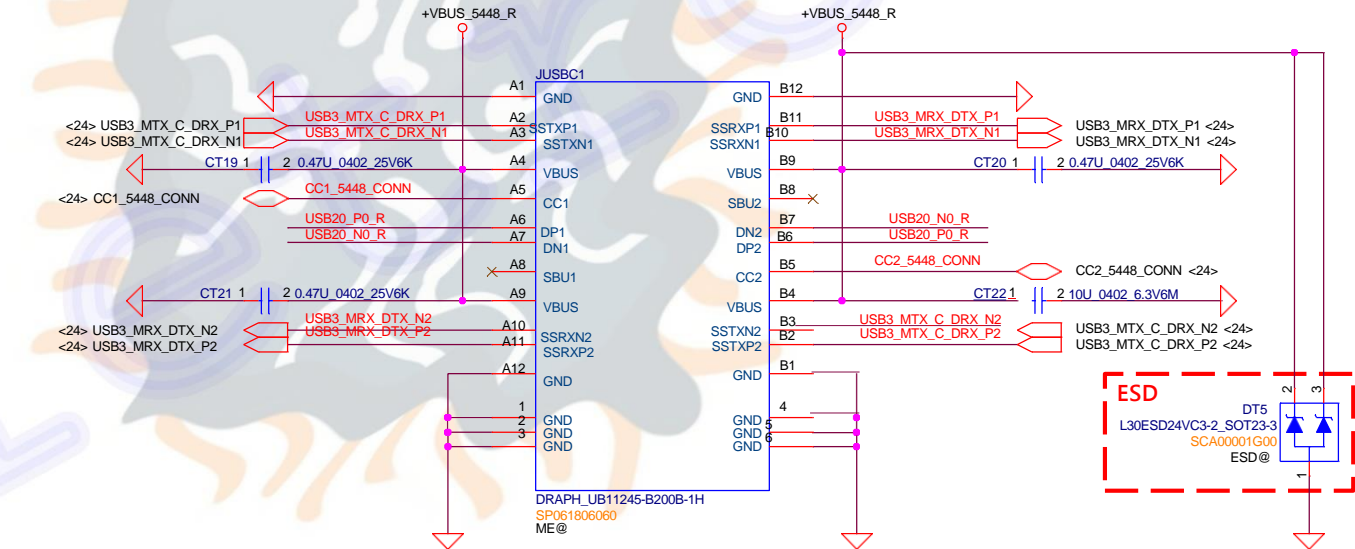
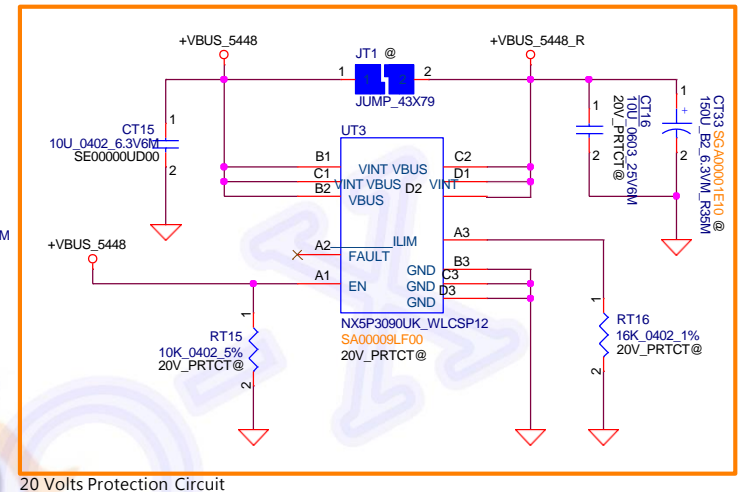
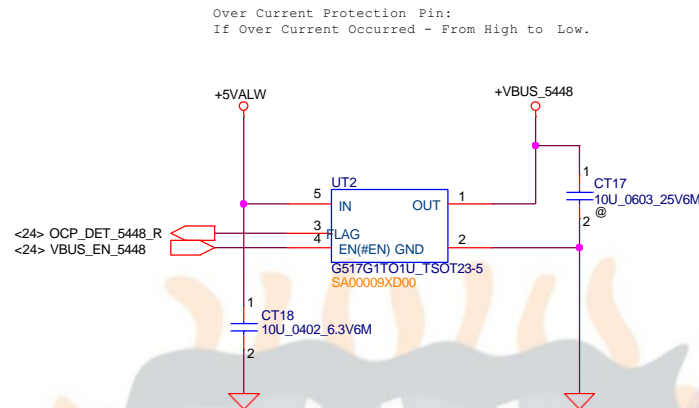
## ESD COMPONENTS



## USB2.0



## TYPE-C CONNECTOR

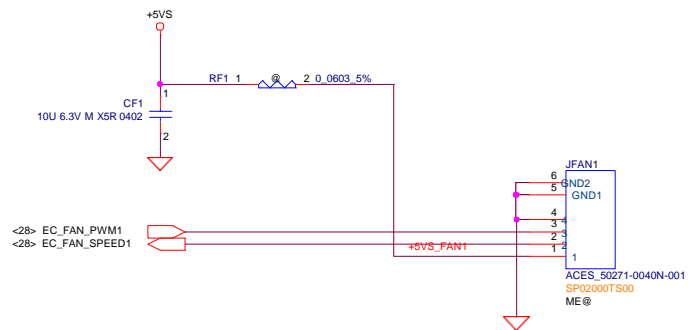


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Size B	Document Number	LA-H131P			Rev 0.4
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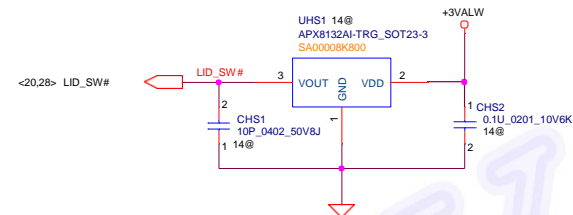




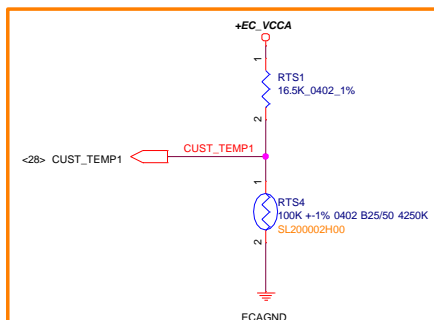
**FAN**



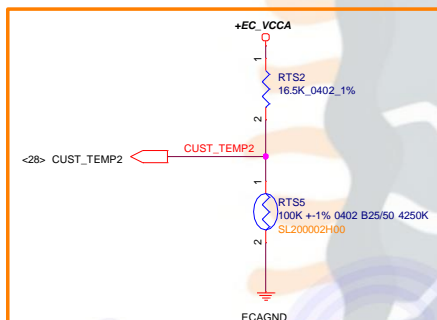
## LID



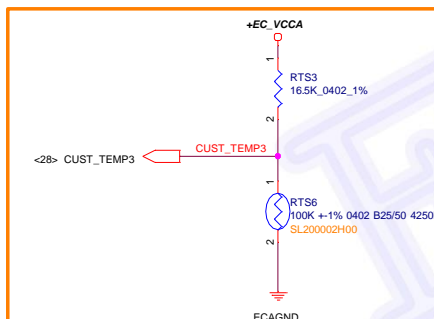
## THERMISTOR



Close to APU

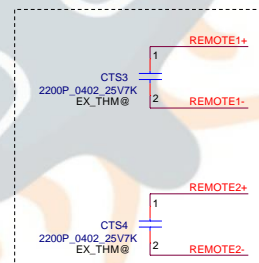
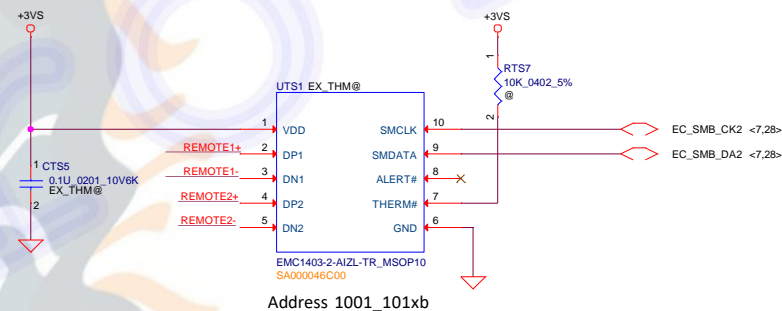


Close to DDR

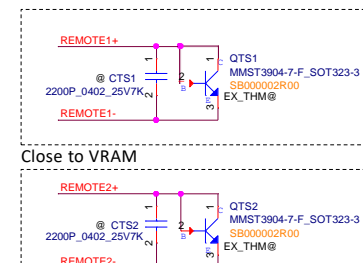


Close to Charger

## THERMAL SENSOR

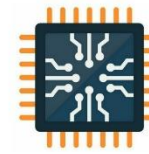


Close to UTS1

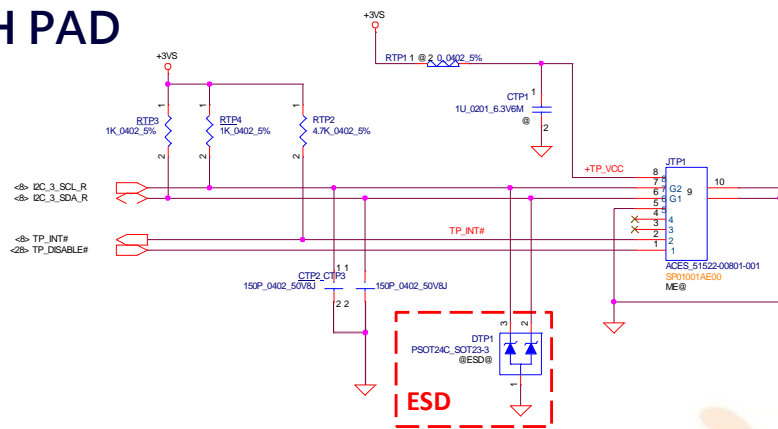


Close to Charger CHOKE

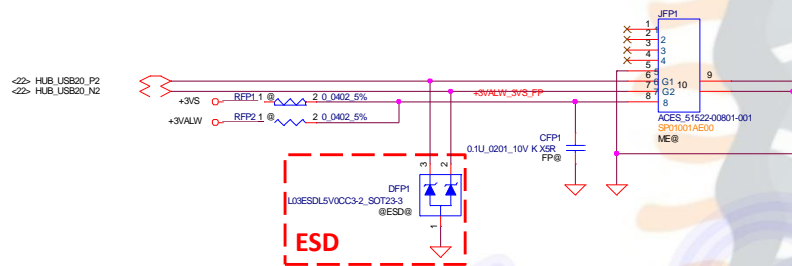
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Date:	Monday, November 05 2018	Sheet	26 of 48		



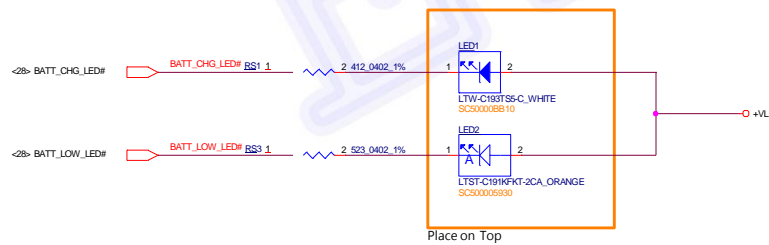
# TOUCH PAD



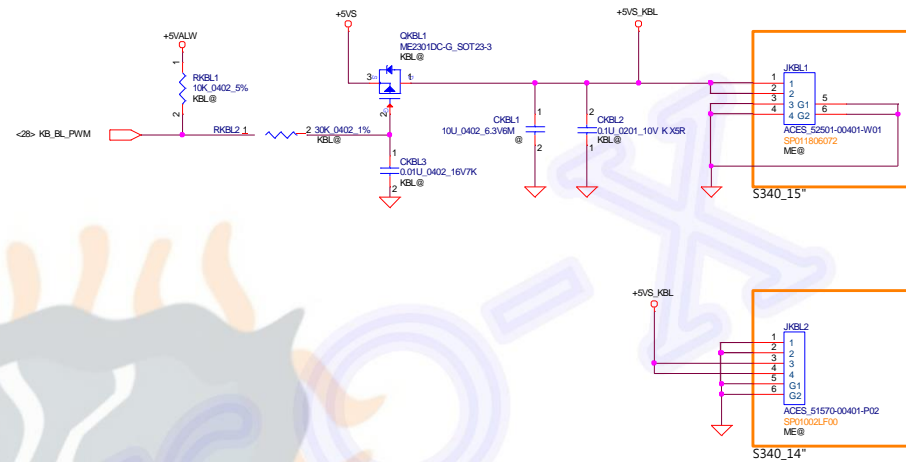
# FINGER PRINTER (RESERVED)



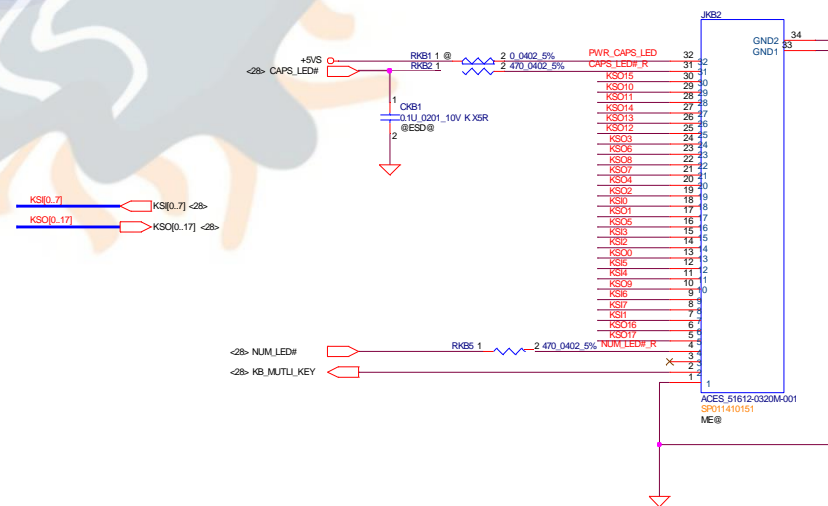
# BATTERY LED



# KEYBOARD BACKLIGHT



# KEYBOARD



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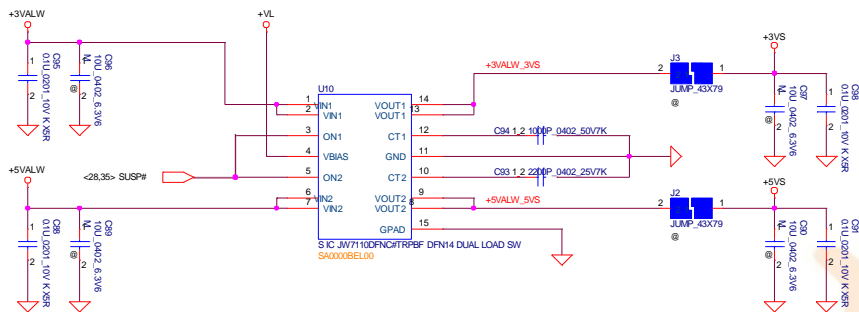


# Eletro-X

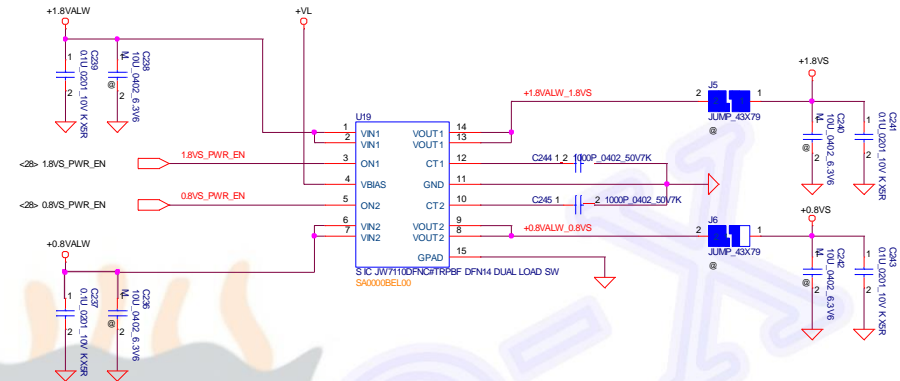


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Printed: Monday, November 02, 2010			Drawn: 02-01-2010		

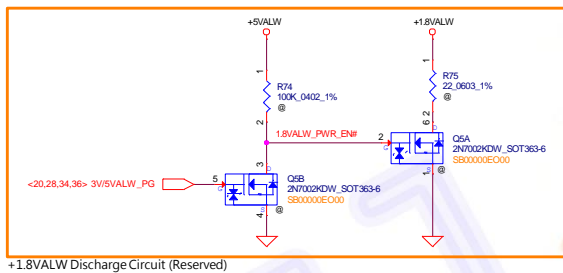
## +3VALW to +3VS / +5VALW to +5VS



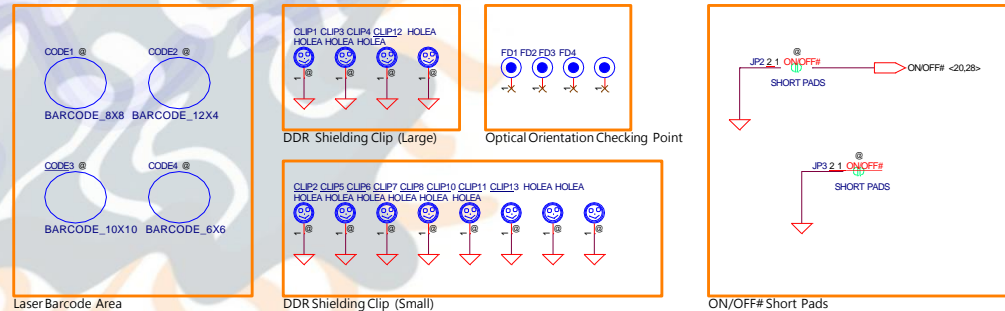
## +1.8VALW to +1.8VS / +0.8VALW to +0.8VS



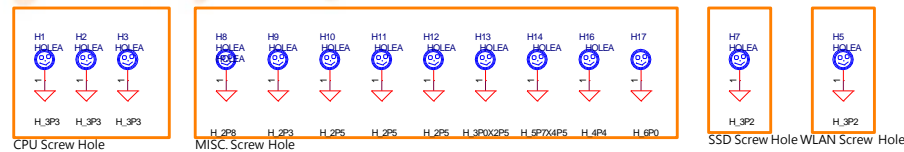
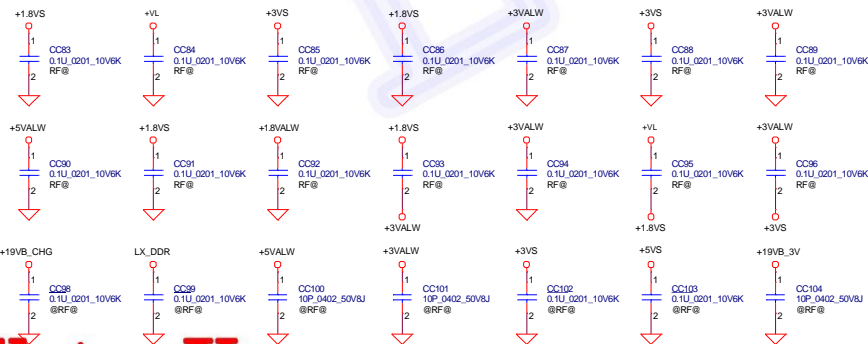
## DISCHARGE CIRCUIT



## MISC.



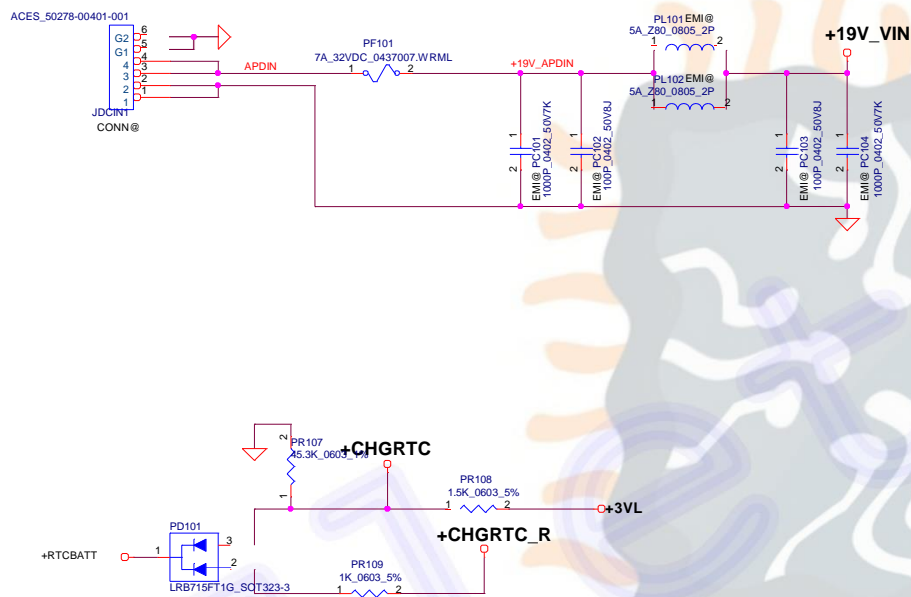
## RF - BY PASS / CROSS MOAT CAPS



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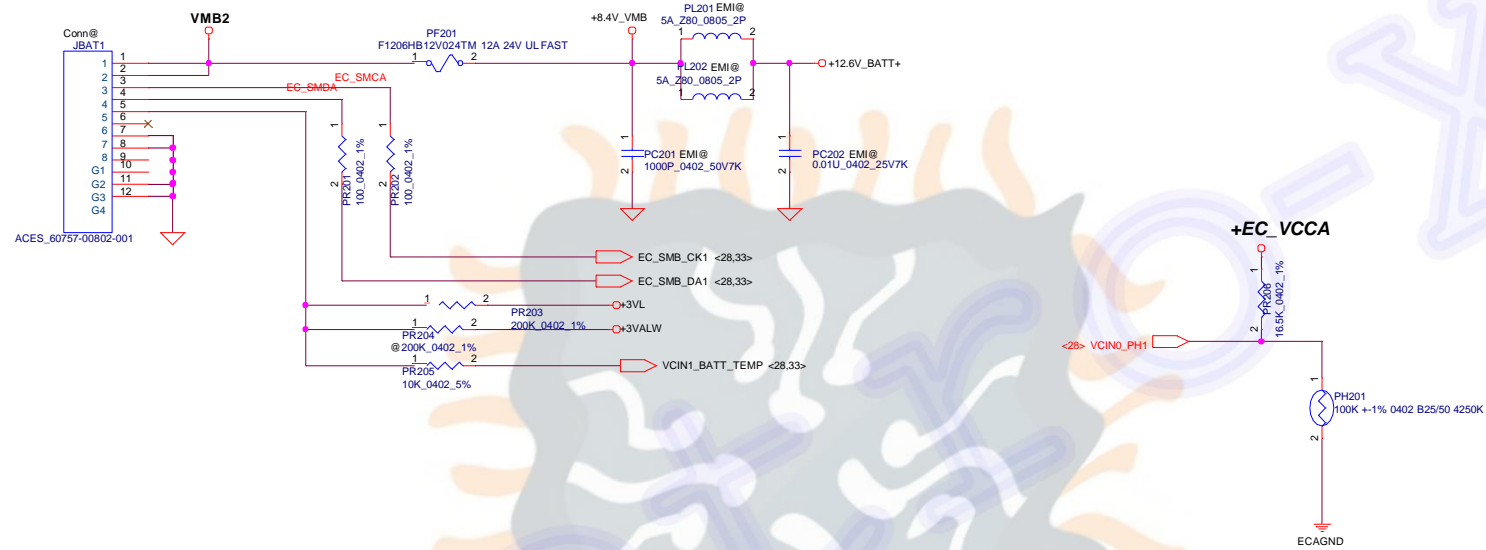




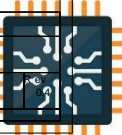


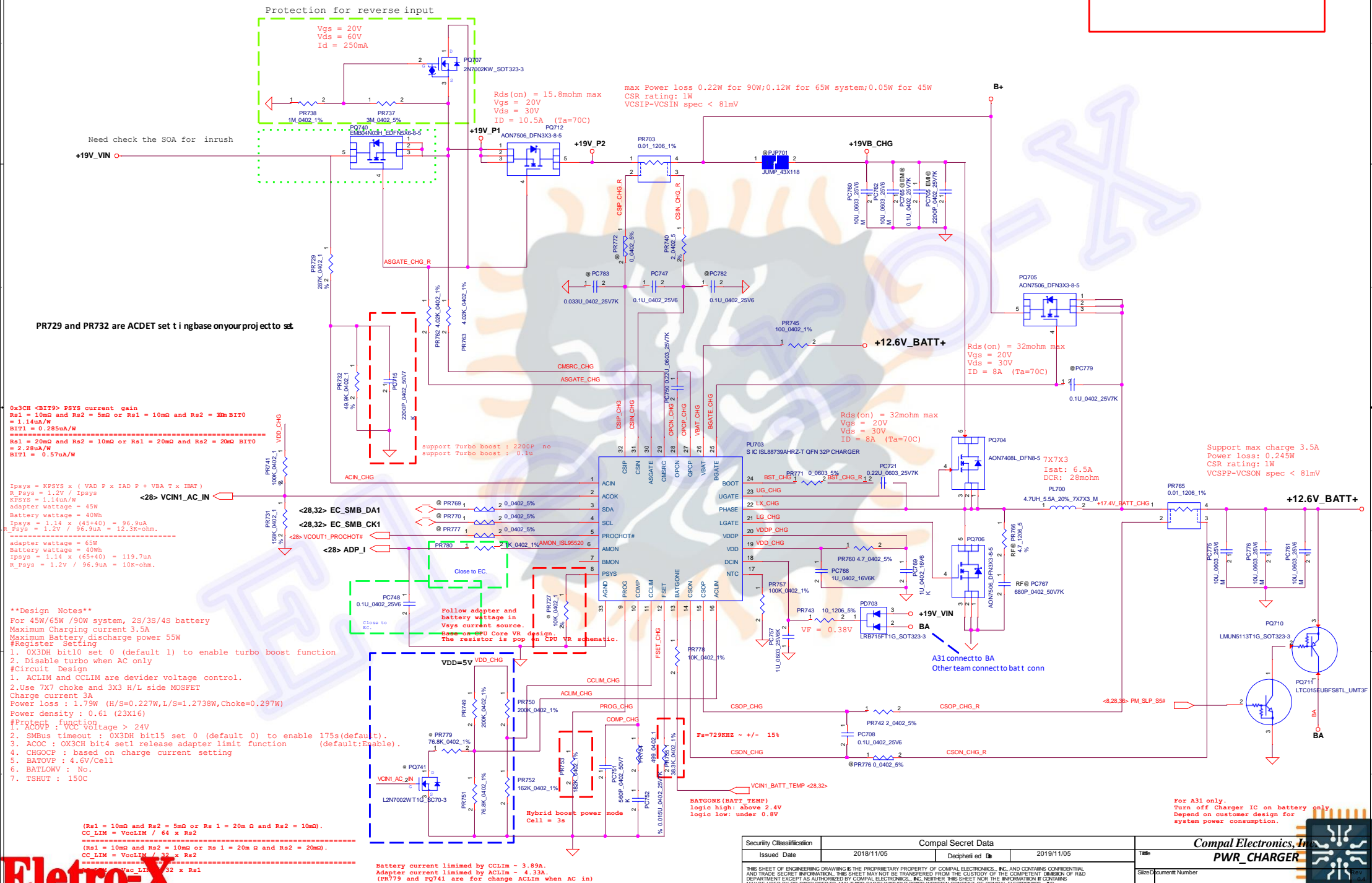
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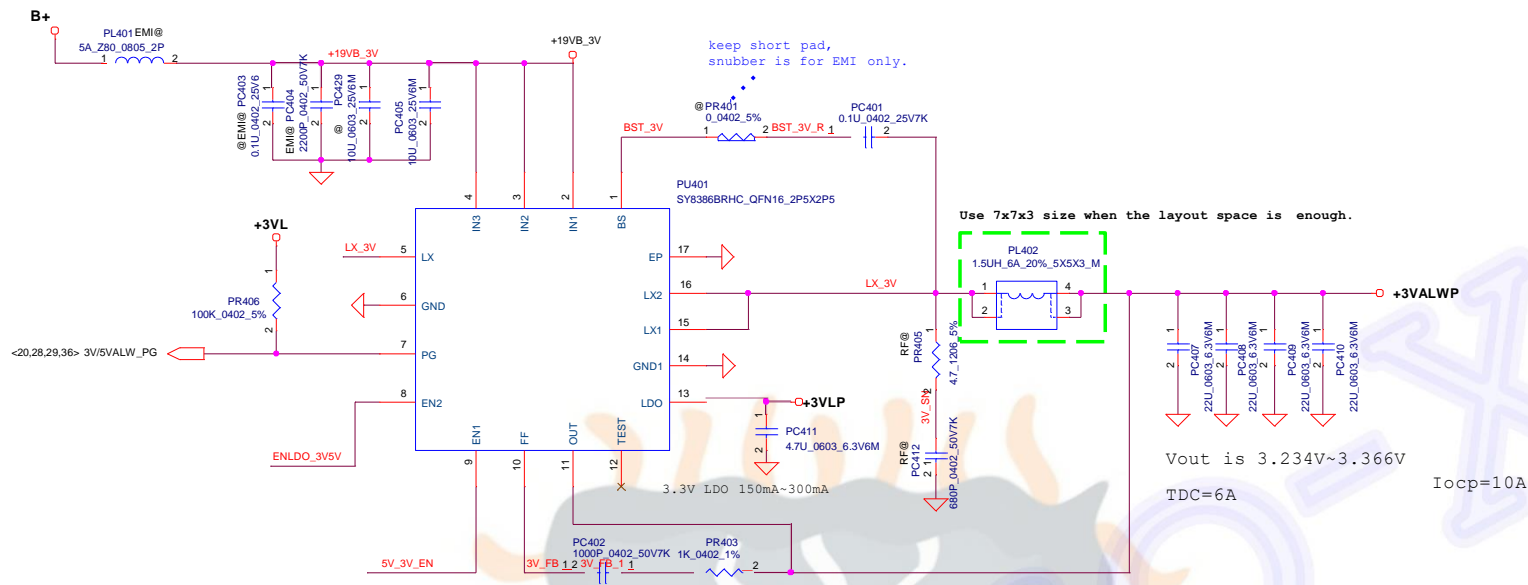




PH201 under CPU bottom side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C







Check pull up resistor of SPOK at HW side

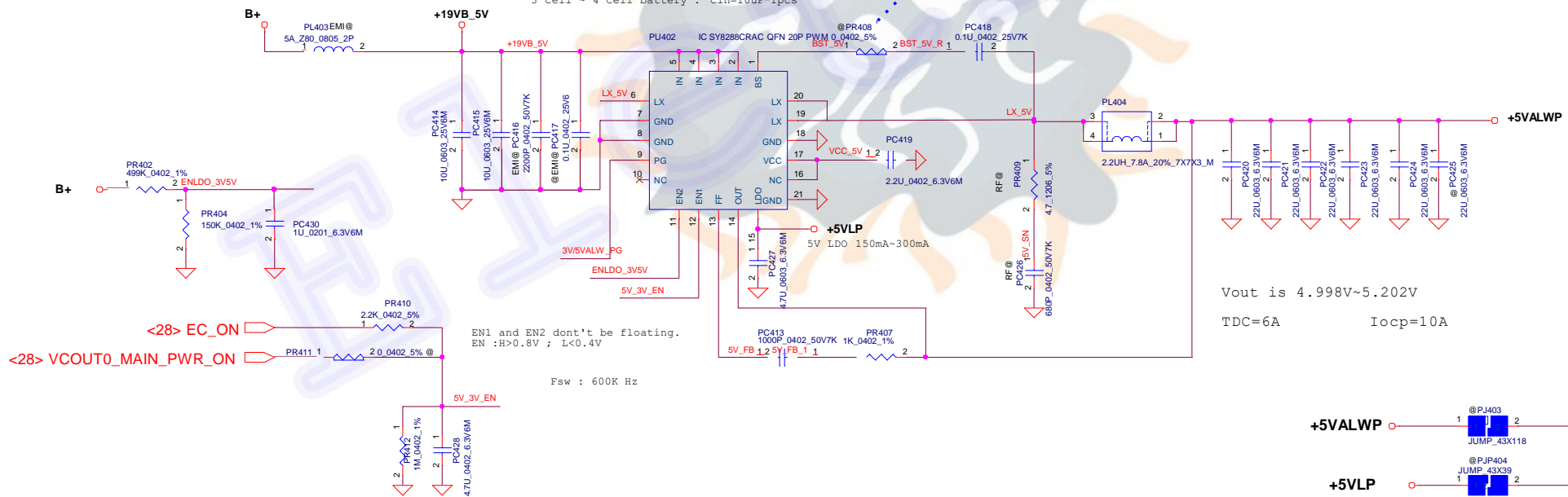
EN1 and EN2 don't be floating.  
EN :H>0.8V ; L<0.4V

Fsw = 600K Hz

Module model information  
SY8286C\_V3\_single.mdd  
SY8286C\_V3\_dual.mdd

+3VALWP @PJ401 JUMP\_43X118 +3VALW

+3VLP @PJ402 JUMP\_43X39 +3VL



+5VALWP @PJ403 JUMP\_43X118 +5VALW

+5VLP @PJ404 JUMP\_43X39 +5VL

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				Custom	0.4
				Date: Monday, November 05, 2018	Sheet 34 of 46

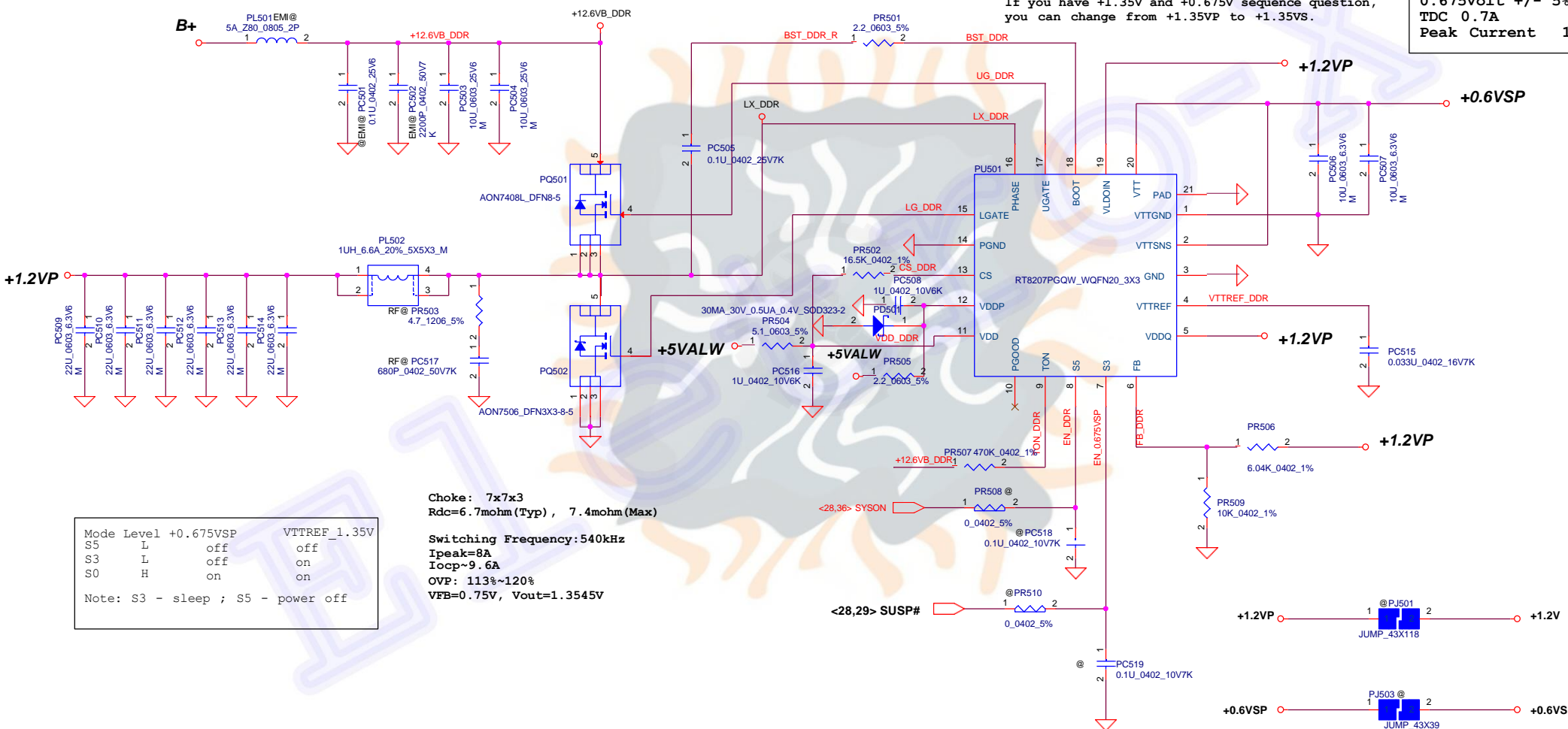


Module Information

RT8207P\_single V3.mdd For Single layer  
RT8207P\_dual V3.mdd For Dual layer

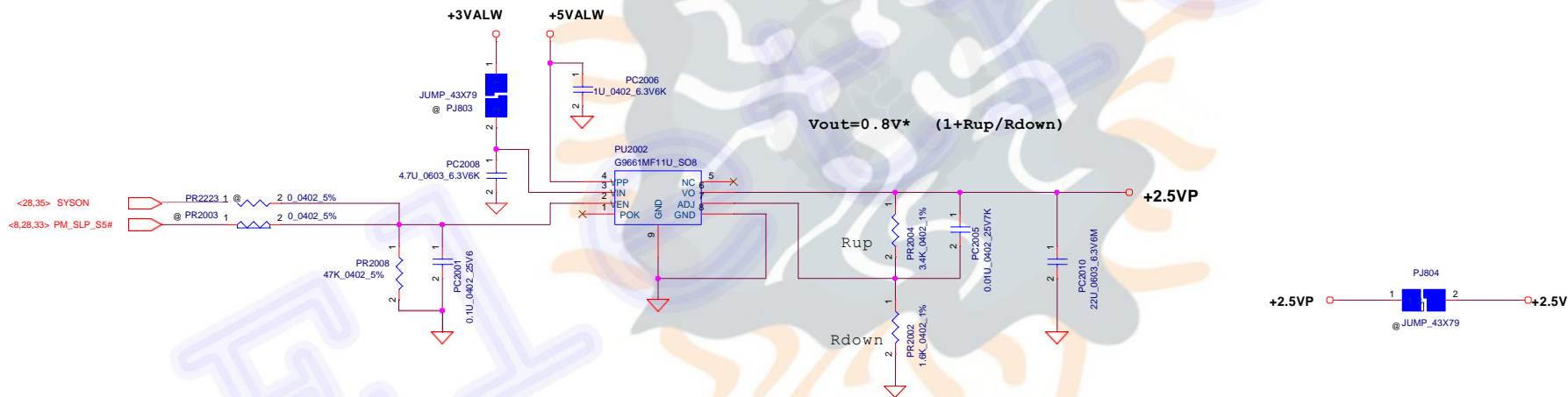
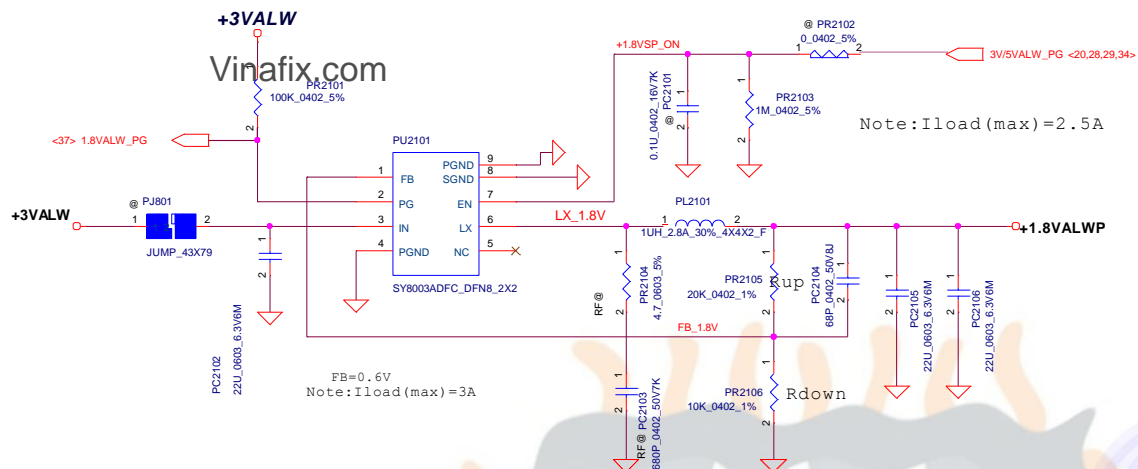
Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

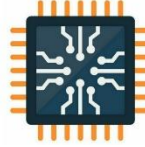


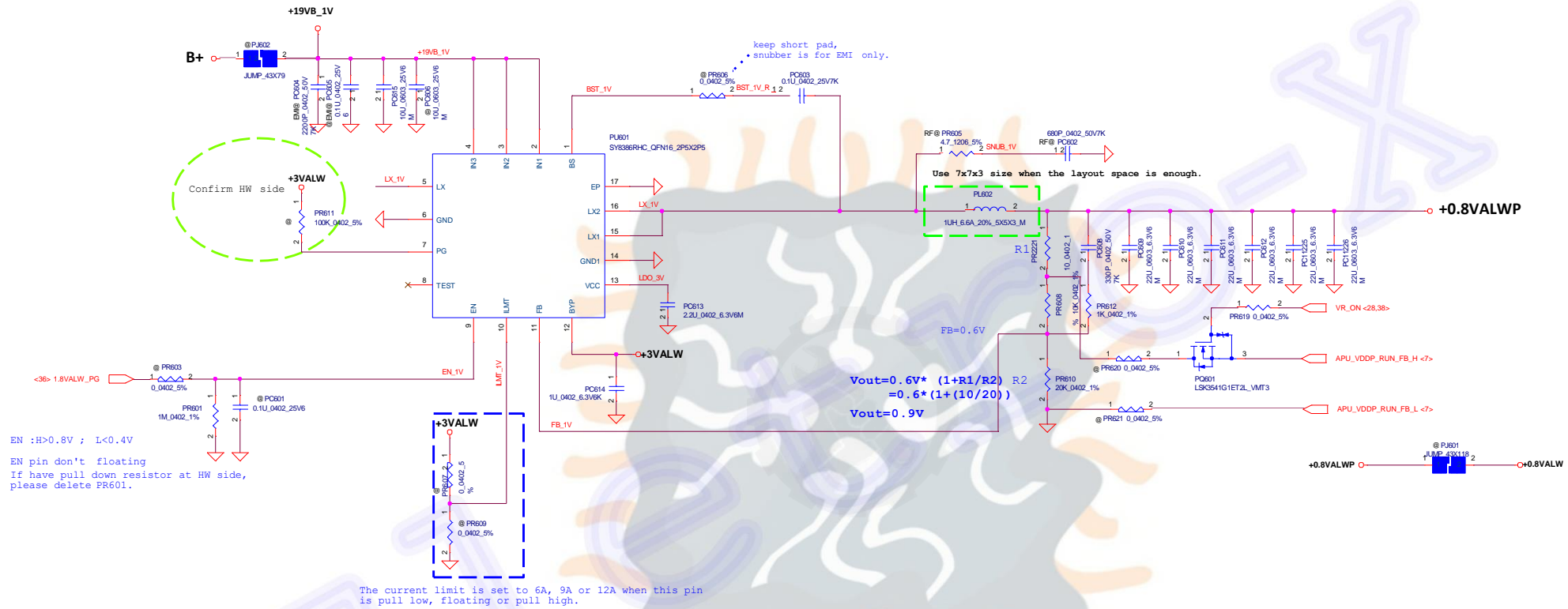
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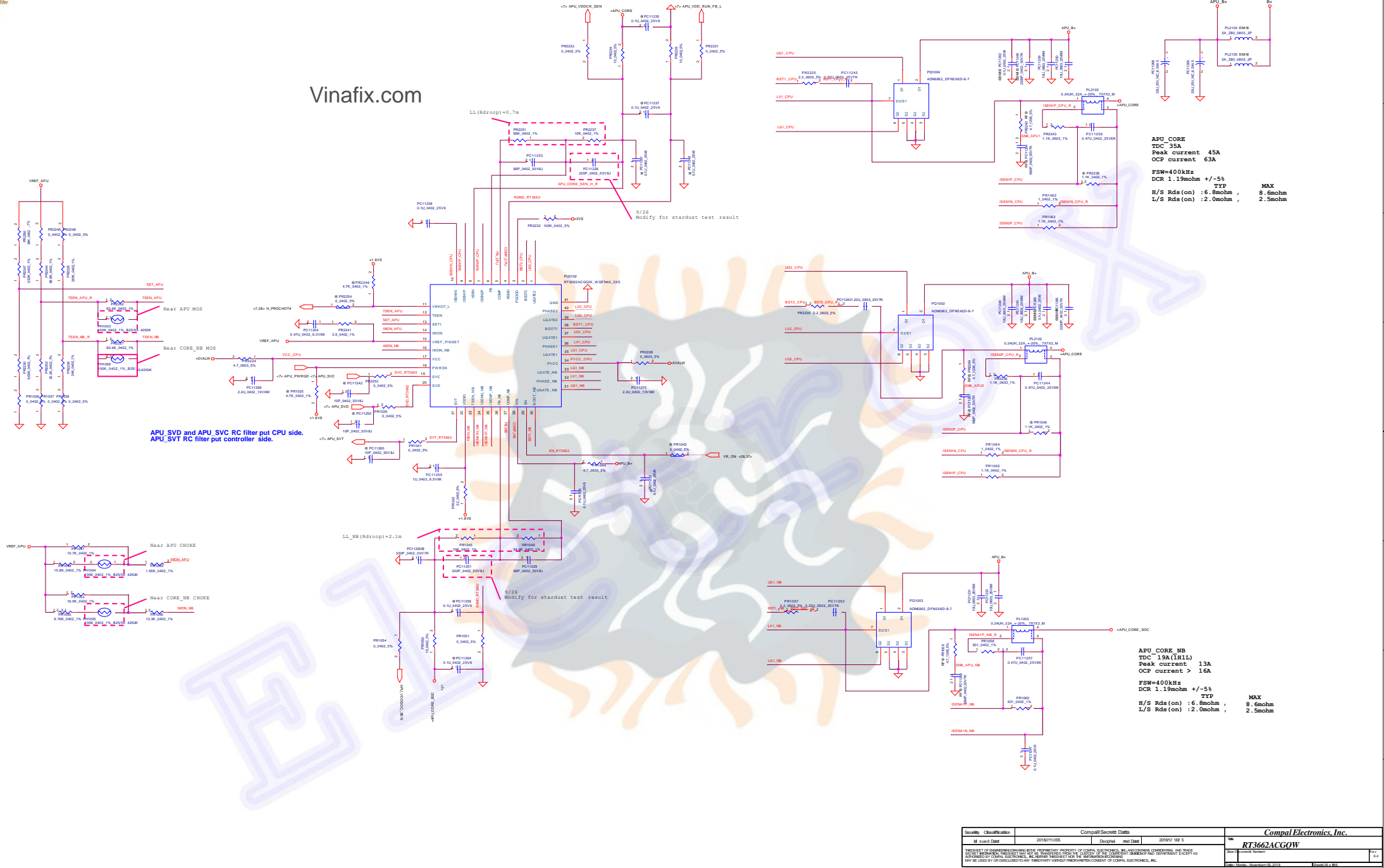
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Size/Document Number		1.2VP/0.6VSP	
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				Customer	R ev 0.4
				Date	Monday, November 05, 2018
				Sheet	36 of 46



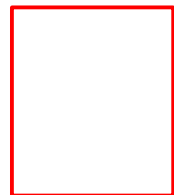




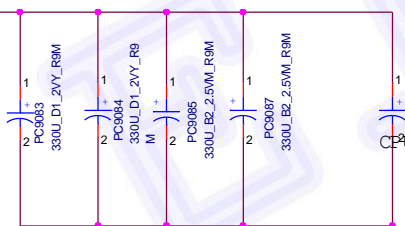
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M		2018/11/15/06		RT362ACGOW	
M		Designed		2019/11/15/06	
M		Designed		2019/11/15/06	
M		Designed		2019/11/15/06	
M		Designed		2019/11/15/06	
M		Designed		2019/11/15/06	
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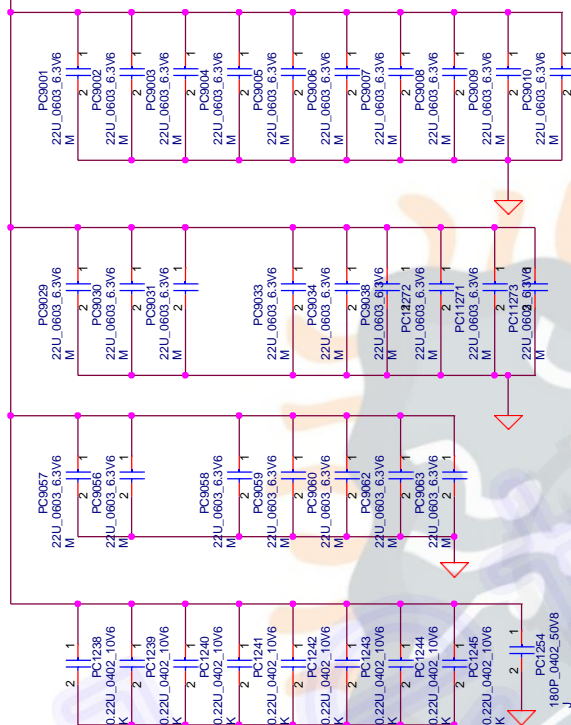


**+APU\_CORE**



near CPU

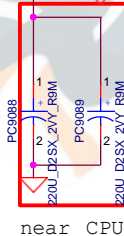
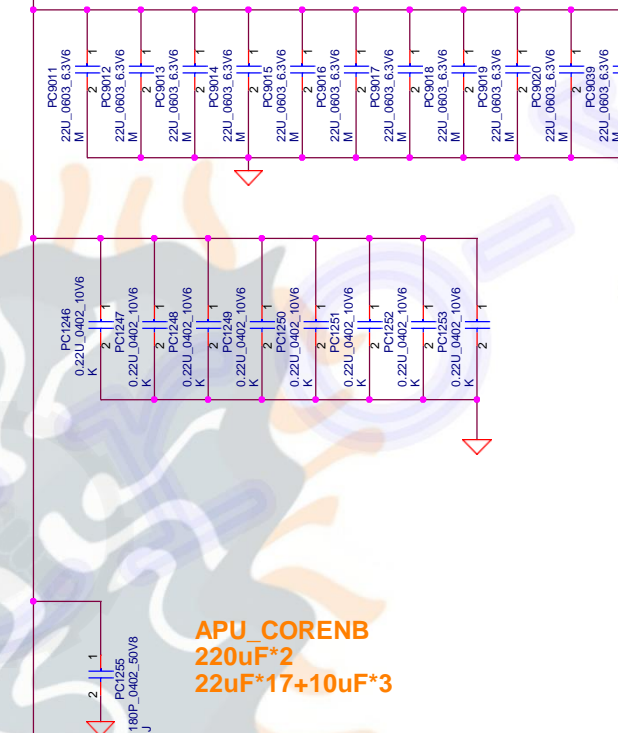
**+APU\_CORE**



**APU\_CORE**  
330uF\*3  
220uF\*1  
22uF\*23

**+APU\_CORE\_SOC**

**+APU\_CORE\_SOC**

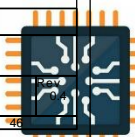


near CPU

**APU\_CORENB**  
220uF\*2  
22uF\*17+10uF\*3

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**Version change list  
(P.I.R. List)**

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for PWR**

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add 0.8VALW remote sense for AM D re que s	P.37	Add transistor PQ601 and 0 ohm PR619,PR620,PR621 for remote sense	2018.08.22	SIV
2	Change common part for 2nd source trail run	P.31	Change PD101 to SCS00008E00	2018.08.22	SIV
3	Change common part for source suggestion	P.38	Change PC11265,PC11266 to SF000007200	2018.08.22	SIV
4	Change DDR choke from 7*7 to 5*5 for common M/B	P.35	Change PL502 to SH00000Z200	2018.08.22	SIV
5	Change VDDP voltage to 0.9Vfor AMD request	P.37	Change PR608 from 6.8K to 10K	2018.09.10	SIV
6	Change CPU_CORE_SOC OCP setting and comparison	P.38	Change PR1046 from 100K to 54.9K Change PR1056 from 23.2K to 13.3K Change PR1053 from 20K to 16.5K Change PR2226 from 316K to 261K Change PR1055 from 6.49K to 9.76K	2018.09.10	SIV
7	Change 0 ohm to R short	P.33	Change PR769,PR770,PR772,PR776 to R short	2018.09.10	SIV

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	21	Change JHP1 symbol	2018/07/03	EVT
2		21	CA25.2,UAUDIO1.22,UAUDIO1.37 change to AGND	2018/07/03	
3	Layout request	25	Swape DT1 pin define	2018/07/03	
4	Common part		UC6,U7,Q3,CD74,CD1,CD2,CD8,CD9,C92,C101,CD10~CD41,C99,Y1 chager to common part	2018/07/04	
5		20	Swape JIO1 pin define	2018/07/04	
6	Layout request	20	Delete D2, R109	2018/07/04	
7	EMI request	25	LT1 change to common part	2018/07/05	
8	Thermal request	26	Delete RTS6,RTS3	2018/07/05	
9	AMD disign guide	24	CT7~CT10 change value	2018/07/05	
10		25	Add CT33	2018/07/09	
11		25	Change JUSBC1 symbol	2018/07/10	
12		27	Delete DFP2	2018/07/10	
13		20	U7 change PN to SA0000B0V00	2018/07/11	
14			JIO1 change to 45 pin	2018/07/12	
15		28	R67 link to GND, R67,R70 un-pop	2018/07/12	
16		8	Delete RC114,RC117	2018/07/12	
17		8	TP_INT# change to AGPIO85	2018/07/12	
18		8,27	Add T21~T24,RC117,RC118,QC3,RTP3,RTP4	2018/07/12	
		17	JSSD1 PCIE pin define	2018/07/16	
			QC3 change to common part	2018/07/16	
			Change LED	2018/07/16	
			CT33 change PN	2018/07/16	
			SATA_ARX_C_DTX_N1,SATA_ARX_C_DTX_P1 swap	2018/07/16	
			Add J2,J3	2018/07/17	

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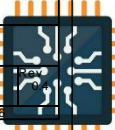
Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	26	Add RTS3, RTS6	2018/07/17	EVT
2		21	Swap U10 pin define	2018/07/17	EVT
3		20	Remove R119, R120, R125, R126. (EMI By-Pass Resistor, USB2.0)	2018/07/18	EVT
4		27	Add Net Name - +TP_VCC, +3VALW_3VS_FP	2018/07/18	EVT
5		10	Remove CC34	2018/07/18	EVT
6		29	Add U19 related circuits.	2018/07/18	EVT
7		29	Modify screw hole H5, H7, H14	2018/07/18	EVT
8		21	Remove CA12, RA22, RA23. (Codec)	2018/07/19	EVT
9		21	Add net name +5VDDA_CODEEC_5VSTB	2018/07/19	EVT
10		20	Replace power rail of USB Charger's power ripple caps to +5VALW.	2018/07/19	EVT
11		20	Replace C51 from 22uF to 4.7uF. (USB Charger)	2018/07/19	EVT
12		14	Add BOM Structure TS@ for R264.	2018/07/19	EVT
13		22	Remove +3VS_DVDD, replace with +3VS_HUB. (UHUB1.21, 27 / CHUB11.1)	2018/07/19	EVT
14		22	Remove RHUB3, RHUB4.	2018/07/19	EVT
15		27	RFP1, CFP1 -> FP@, DFP1 -> @ESD@	2018/07/20	EVT
16		15	Replace JHDMI1 Symbol (DC232007B00)	2018/07/20	EVT
17		29	Remove Clip8	2018/07/20	EVT
18		17	Replace JSSD1 Symbol (SP070018L00), Pin Count different with before	2018/07/20	EVT
19		22	RHBU3~5 -> RHUB3~5, RHBU1 -> RHUB6, RHBU2 -> RHUB7	2018/07/20	EVT
20		8	QC3.2 / QC3.5 -> From +3VALW to +3VS	2018/07/20	EVT
21		20	Swap JIO1 USB3 Pin Define (TX/RX, P/N) -> Total 8 Traces	2018/07/20	EVT
22		17	Remove BOM Structure "SSD@"	2018/07/20	EVT
23		17	Add RSSD4~7	2018/07/20	EVT
24		29	Remove +0.6VS / +0.8VS Discharge Circuits.	2018/07/23	EVT

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	17	Add RSSD8, RSSD9	2018/07/23	EVT
2		29	Replace Clip9 with Clip8 (Remove Clip9)	2018/07/23	EVT
3		15	Swap DH2, DH3 nets to reduce via	2018/07/23	EVT
4		22	Replace Y1 Part Number. (to SJ10000C210)	2018/07/23	EVT
5		29	Add CC83 ~ CC96 (RF By Pass / Cross Moat Caps)	2018/07/23	EVT
6		27	Replace Keyboard Power Rail from +5VALW to +5VS	2018/07/24	EVT
7		8	Re-Name MODEL ID0 / ID1 with MODEL_ID / MIC_SELECT	2018/07/25	EVT
8		8	Update Memory ID Matrix	2018/07/25	EVT
9		3	Update Note List Page	2018/07/25	EVT
10		19	Remove T2408 BOM Structure (TP@)	2018/07/25	EVT
11		29	Pop CC83~CC96 (RF@)	2018/07/25	EVT
12		14	Remove R264, C230 BOM Structure (TS@)	2018/07/25	EVT
13		21	DA1.4 / DA1.6 Pin Swap	2018/07/26	EVT
14		15	Swap DH1.4 / 7 to DH1.5 / 6	2018/07/26	EVT
15		20	Update U7 Part Description (USB Charger)	2018/07/27	EVT
16		25	Update JUSBC1 footprint with DRAPH_UB11245-B200B-1H_24P-S	2018/07/27	EVT
17		9	Replace ROM (UC2) Part Number to SA00008K400	2018/08/06	EVT
18		27	Replace CTP1 from 0402 to 0201 (EVT Gerber Keep 0402)	2018/08/06	EVT
19		27	Replace CTP1 from 0201 to 0402	2018/08/08	EVT2
20		13	JDIMM1.162, 1.165 -> 1.149, 1.157	2018/08/08	EVT2
21		21	Replace RA13, RA14 footprint from 0603 to 0402	2018/08/09	DVT
22		27	Replace CTP1 from 0402 to 0201	2018/08/09	DVT
23		25	Replace CT33 part number with SGA00001E10	2018/08/10	DVT
24		29	Add screw hole H16, H17	2018/08/16	DVT

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	29	Change Clip2 to small size	2018/08/16	DVT
2		26	Add UHS1, CHS1, CHS2 for LID switch	2018/08/16	DVT
3		17	Delete RSSD4~RSSD7 for PCIE/SATA MUX debug	2018/08/20	DVT
4	Support type2 APU	9,24	Change typeC USB3 to port0	2018/08/20	DVT
5		22	Reserve RHUB10~RHUB13 for touch scerrn co-lay	2018/08/20	DVT
6	Power request	7,37	VSS_SENSE_B conntector to 1.8VALW	2018/08/21	DVT
7	Audio request	21	Swap SPK pin define	2018/08/21	DVT
8		28	R55 change to 15@	2018/08/23	DVT
9		26	Reserve Thermal Sensor. (UTS1 and related circuits)	2018/08/23	DVT
10		21	Swap HGND A& HGND B	2018/08/25	DVT
11	HDMI issue	07	RC17 change to mount RC18 to un-mount	2018/08/28	DVT
12			RC117/RC118/RTP1/RF1/R3/RHD5/R53/R111/ R264/RA12/RWL1/RSSD1 Change to R-short	2018/08/28	DVT
13		29	Del U8/C85/C86/C87/J1/R72/C92/U18/C99/C100/C101/R73/J4	2018/08/31	DVT
14		27	Del RKB3/RKB4	2018/08/31	DVT
15		27	Add JKBL2 for KBL 14"/15" co-lay	2018/09/02	DVT
16	ESD Request	5	Reserve CC97	2018/09/06	DVT
17		22	Replace USB2.0 HUB from Port0 to Port4	2018/09/06	DVT
18		25	Replace USB2.0 Type-C from Port4 to Port0	2018/09/06	DVT
19		28	R55 -> Always Pop (No matter 14" or 15")	2018/09/06	DVT
20		29	Replace CLIP12 with bigger size	2018/09/06	DVT
21		29	Modify H8 / H9 screw hole size	2018/09/06	DVT
22		27	Replace RFP1 with R-Short	2018/09/06	DVT
23		17	Remove RSSD4~7	2018/09/06	DVT
24		26	Add BOM Structure 14@ for 14" LID Switch (UHS1)	2018/09/07	DVT

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	22	Add BOM Structure HUB@	2018/09/07	DVT
2		8	Add BOM Structure NO_OBR@	2018/09/07	DVT
3		12	Add BOM Structure OBR@	2018/09/07	DVT
4		20	Un-Mount C48 / C49	2018/09/07	DVT
5		25	Un-Mount CT33 / Replace CT22 from 0.47uF to 10uF	2018/09/07	DVT
6		29	Mount C244, C245	2018/09/07	DVT
7	Cost Down Item	10	Un-Mount CC56, CC60, CC61, CC62, CC65, CC79, CC75, C1	2018/09/07	DVT
8	Cost Down Item	17	Un-Mount CSSD4, CSSD5	2018/09/07	DVT
9	Cost Down Item	13	Un-Mount CD76, CD79	2018/09/07	DVT
10	Cost Down Item	12	Un-Mount CD29, CD30, CD44, CD45, CD50, CD52	2018/09/07	DVT
11	Cost Down Item	13	Replace CD55, CD58, CD59, CD65, CD66, CD67 with NO_OBR@	2018/09/07	DVT
12		8	MODEL_ID -> RC112 (15@) / RC115 (14@)	2018/09/07	DVT
13	Fine Tune Crystal Caps	9	CC27/CC28 -> Replace with 4.7pF (Vendor Suggestion: 3.9pF)	2018/09/11	DVT
14	Fine Tune Crystal Caps	9	CC30/CC31 -> Replace with 10pF	2018/09/11	DVT
15	Fine Tune Crystal Caps	22	CHUB9 / CHUB10 -> Replace with 33pF (Not Replace it Yet)	2018/09/11	DVT
16		21	DA3 / DA4 -> Replace with SCA00004300	2018/09/11	DVT
17		27	Replace RTP3 / RTP4 with 1K Ohm	2018/09/14	DVT
18		27	Replace CTP2 / CTP3 with 150pF	2018/09/14	DVT
19		3	Add DAZ and PR APU P/N, Modify DA BOM Structure	2018/10/03	PVT
20		28	Replace KB_MUTLI_KEY - Pull Up +3VALW to +3VL	2018/10/03	PVT
21		29	Update CC94 cross moat caps power rail	2018/10/08	PVT
22			0 Ohm to R-Short -> R2, R9, RSSD2, RC64	2018/10/08	PVT
23	ESD Request	25	Remove DT3, Combine CC1/CC2 to DT4	2018/10/18	PVT
24	ESD Request	21	Add C246 (PLUG_IN)	2018/10/18	PVT

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Vinafix.com	5	RC2 -> OBR@	2018/10/18	PVT
2		29	Add 6x6 Laser Barcode Area	2018/10/19	PVT
3	ESD Request	21	Remove C246, Rename it to CA30 (0.1uF), Reserve CA31	2018/10/22	PVT
4		25	DT4 Pin1 & 6 Swap	2018/10/23	PVT
5		27	Swap JKBL1 Pin Define	2018/10/24	PVT
6	ESD Request	21	CA16 / CA17 - 470pF to 1000pF, Remove CA31 & RA24 (Replace with CA30)	2018/10/26	PVT
7		7	JHDT1 Footprint add "-NPM" -> SAMTE_ASP-136446-07-B_20P-T-NPM	2018/10/29	PVT
8	RF Request	29	Reserve CC98 ~ CC104 By-Pass Caps	2018/10/29	PVT
9	ESD Request	13	Pop CD69	2018/10/29	PVT
10		9	Replace ROM (UC2) Main Source with SA0000BJU00 (XMC)	2018/10/30	PVT
11		29	Replace Dual Load Switch (U10, U19) Main Source with SA0000BEL00	2018/10/30	PVT
12		29	Replace Small Clip Footprint (EMIST_SUL-15A3M_1P) - x8 PCS	2018/10/30	PVT
13		29	CC99 / CC102 / CC103 Replace with 0201, CC99 Power Replace with LX_DDR	2018/10/30	PVT
14		23	Add Type-C USB3.0 Re-Driver Related Circuit (RT17~39, CT34~41, UT4)	2018/10/31	PVT
15		29	Replace CC98 with 0201 footprint	2018/11/01	PVT
16		23	Modily BOM Structure of USB3 Re-Driver	2018/11/01	PVT
17		7	Reserve QC4	2018/11/01	PVT
18		25	Mount CT15	2018/11/05	PVT
19					
20					
21					
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